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VLSI Architecture of Polar Encoding and Decoding for 5G Applications

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***Abstract*— Polar codes, recognized as the first error-correcting codes to achieve the Shannon capacity, have gained significant attention in the field of wireless communication, particularly in the context of 5G applications. Their adoption by the 3GPP as the channel coding scheme for the 5G enhanced mobile broadband (eMBB) control channels highlights their critical role in achieving ultra-reliable and low-latency communication. This paper explores the VLSI architecture of polar encoding and decoding systems optimized for 5G applications. By leveraging the inherent recursive structure of polar codes, we propose efficient hardware designs that minimize latency, improve throughput, and optimize power consumption. This paper focuses on implementing polar encoding and decoding. Simulation results present the improvement in the performance metrics.**

Keywords*— VLSI, FPGA, IOT, 5G, AI, Xilinx ISE, Polar Code.

I. INTRODUCTION

The advent of 5G technology has revolutionized wireless communication, enabling faster data rates, lower latency, and enhanced connectivity for applications ranging from autonomous vehicles to the Internet of Things (IoT). To support these ambitious goals, robust error correction techniques are essential to ensure reliable data transmission over noisy communication channels [1]. Among various error-correcting codes, polar codes have emerged as a groundbreaking solution, being the first codes to achieve Shannon's channel capacity under low-complexity decoding algorithms. Their selection by the 3GPP for 5G New Radio (NR) control channels underscores their importance in achieving the performance benchmarks set by modern communication standards [2].

Polar codes operate on the principle of channel polarization, wherein the reliability of individual bit channels is maximized through a recursive process. This enables a subset of bit channels to be utilized for data transmission, while the others are frozen to known values. While theoretically optimal, practical implementation of polar codes poses significant challenges, particularly in terms of hardware design for encoding and decoding [3]. The recursive structure of polar codes, while advantageous for theoretical analysis, introduces complexity in real-time applications, necessitating the development of efficient Very-Large-Scale Integration (VLSI) architectures [4].

The encoder for polar codes involves matrix-vector multiplication using a generator matrix, which is derived from the Kronecker product of smaller matrices. This operation, though conceptually straightforward, becomes computationally intensive for large block lengths. On the other hand, decoding is even more challenging due to the iterative nature of algorithms like successive cancellation (SC) and successive cancellation list (SCL) [5]. The decoding process involves traversing a binary tree, where decisions made at each node depend on previously decoded bits. While SCL decoding improves performance by considering multiple decoding paths, it significantly increases hardware complexity and memory requirements [6].

To address these challenges, this paper investigates the VLSI design of polar encoding and decoding architectures tailored for 5G applications. The primary goal is to achieve a balance between hardware efficiency, latency, and error-correction performance. Key contributions include leveraging

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pipelining and parallelism to accelerate encoding and decoding processes, optimizing memory usage to reduce chip area, and implementing hybrid decoding strategies that combine SC and SCL decoding for improved performance [7][8].

II. LITERATURE SURVEY

D. Kam et al. [1] introduce an extraordinary failure intricacy combining activity that can increase the number of equal elements to facilitate the comprehension of tree-level parallelism. We also modify the previous pruning method to reduce the number of visited nodes in the same SC interpreting circumstance. Similarly, a unique equal-half aggregate minicomputer (PSC) design is capable of updating incomplete total registers with numerous decoded bits in a single processing cycle.

A. E. Krylov et al.[2] suggest a low-latency and low-intricacy apparatus engineering for PQ that is dependent on the systolic sorter and enhanced by the arrangement of natives. The reproduction results indicate that a minimal amount of BER degradation is observed when compared to optimal full-scale organising organisations.

The initial apparatus engineering for ORBGRAND, as reported by S. M. Abbas et al.,[3], achieves a typical throughput of up to 42.5 Gbps for a code length of 128 at an SNR of 10 dB. Furthermore, the proposed apparatus is capable of decoding any code, provided that the length and rate requirements are met. In contrast to the state-of-the-art rapid potent successive cancellation flip decoder (rapid DSCF) that employs a 5G polar (128,105) code, the proposed VLSI implementation maintains comparable decoding performance while achieving a 49× increase in average throughput.

A hub-based cyclic overt repetitiveness check (CRC)-aided successive cancellation list (NRB CA-SCL) polar decoder engineering is presented by H. - Y. Lee et al.,[4]. The quantity of growing ways is determined by hub unwavering quality, and a need-based sorter is developed to reduce the number of organising cycles. The hub processor is anticipated to reduce the amount of work required for organising by producing the extending sections using disconnected rotating designs. We also suggest a post-processing strategy that enhances the rate of error execution for the NRB CA-SCL decoders.

In order to reduce the number of Handling Components (PEs) to only log_2N for an N-digit code, W. Tan et al.[5] proposed engineering that adapts the optimisation strategies from Quick Fourier Change (FFT) and employs undeniable level change techniques, such as collapsing, pipelining, and retiming. Additionally, the PE plan employs the pre-calculation strategy to enable the simultaneous unravelling of two parts. We also suggest a modified circle-based moving register to further reduce the use of delay components. Our trial results indicate that our engineering reduces the standard in region utilisation and region time item by 98.86% and 77.71%, respectively, when N = 1024, in comparison to the previous works.

In this article, C. Ji et al.[6] have proposed autogeneration, which is capable of decoding the age equation of BPDs to productive equipment executions. Two BPD models have been provided for a variety of prerequisites: 1) a minimal expense decoder (Type-I) and 2) a high-throughput decoder (Type-II). The autogeneration of them can maintain a variety of code rates, code lengths, and parallelisms. The results of the blend indicate that Type-I and Type-II SC decoders provide a higher throughput and equipment productivity than the cutting-edge (SOA) SC decoders.

The general setting is shown to preserve the symmetric property and the debasement relationship, which provides the potential for a modification of Tal-Vardy's technique, as demonstrated by W. Tune et al.[7]. The reenactment results clearly demonstrate that the proposed new strategies have been instrumental in the further development of error execution during reordering. In the same vein, an ingenious encoding apparatus design is suggested, which accommodates penetrating and shortening modes.

The novel qualities of channel accomplishing property render polar encoding the most effective among the various successful encoding methods, as per R. Kavipriya et al.[8]. The coding scheme selected by the Third Generation Partnership Project (3GPP) is binary code, as it has been designed with the fifth-generation remote system in mind. The research that is currently underway is focused on the use of polar codes within the MIMO framework. The polar encoder is fundamentally designed to have a high handling speed in comparison to other methods.

In the handling component (PE) unit of the conviction spread polar decoder, R. Shrestha et al.[9] proposed a strategy for registering logarithmic-probability proportion (LLR) messages that is reliant on two's complement representation of LLR values. Additionally, an alternative PE-design has been implemented in comparison to this method, which necessitates less equipment and has a more restricted fundamental way

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delay, resulting in a higher clock frequency and capacity. We have integrated these PE units into the design of a single-segment-based unidirectional conviction-engendering polar-decoder that employs the full circle ticketing to decode the polar code of 1024 code-length and 1/2 code rate.

A productive design for the successive-cancellation polar decoder is presented by H. Y. Yoon et al.,[10] presented designed in accordance with the standard tree design, which includes multibit translation and covered booking. However, the design is summarised with respect to high-radix handling, which involves the management of a few successive radix-2 bits within a cycle. The complexity and throughput of the combined tree engineering are determined in light of the extensive radix management.

III. METHODOLOGY

The methodology is explained by the following flow chart-

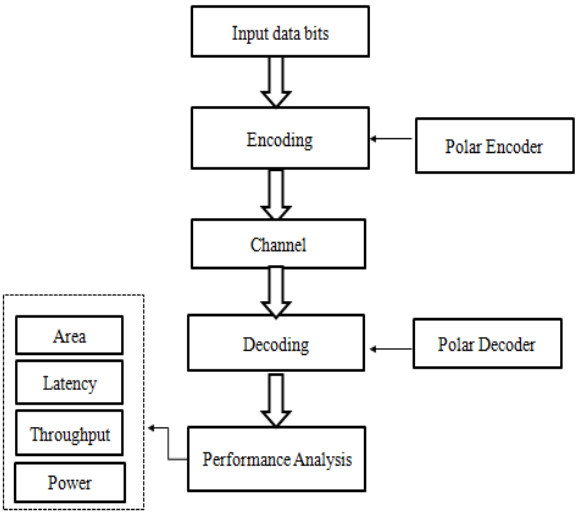

Figure 1: Flow Chart

The provided flowchart outlines the process involved in the VLSI architecture for implementing polar encoding and decoding, along with its performance evaluation.

1. **Input Data Bits**: This is the starting point of the process, where a sequence of data bits is provided as input. These data bits represent the information that needs to be transmitted over a communication channel.
2. **Encoding**: The data bits are passed through the Polar Encoder, where polar encoding is applied. This step involves generating the encoded data using the polar code's generator matrix, ensuring the data is more resilient to errors during transmission. Polar encoding leverages the channel polarization technique to allocate bits to either reliable or frozen channels.
3. **Channel**: After encoding, the data is transmitted over the communication channel. In this stage, the encoded data may encounter noise, interference, or other impairments inherent to the communication medium. This represents a realistic scenario in wireless communication, such as in 5G networks.
4. **Decoding**: The received data is processed by the Polar Decoder, which attempts to recover the original data bits by applying decoding algorithms. Common techniques include Successive Cancellation (SC) decoding, Successive Cancellation List (SCL) decoding, or Belief Propagation (BP) decoding. The decoder aims to mitigate the effects of noise and retrieve the transmitted information accurately.
5. **Performance Analysis**: Once decoding is complete, the system's performance is evaluated based on critical metrics:
   Area: Refers to the chip area consumed by the VLSI architecture. Minimizing area is essential for reducing manufacturing costs and enabling integration into compact devices.
   Latency: Measures the time taken for encoding, transmission, and decoding. Low latency is crucial for real-time applications, especially in 5G control channels.
   Throughput: Refers to the rate at which data can be processed. High throughput ensures the system can handle large volumes of data efficiently.
   Power: Represents the power consumption of the hardware. Optimized power consumption is vital for energy-efficient designs, particularly in portable and IoT devices.

IV. SIMULATION AND RESULTS

The proposed polar code is implemented and simulated by using the Xilinx ISE 14.7 software, The Isim simulator is used to check the results validity in test bench.

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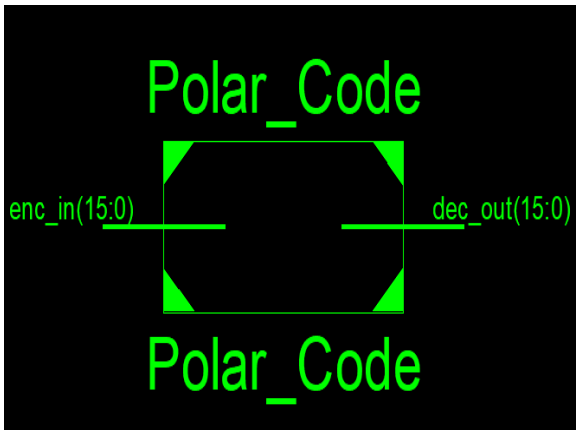

Figure 2: Top view of polar code

Figure 2 is showing the top view of the proposed code, which includes the polar encoder, decoder and channel.

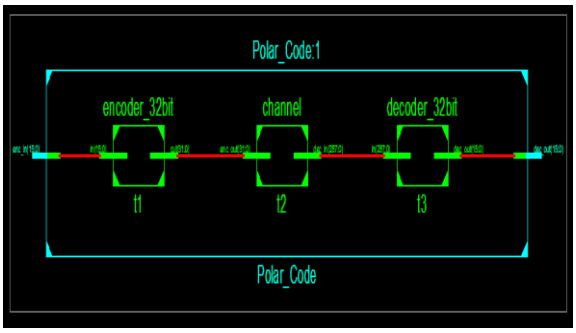

Figure 3: Polar code steps

Polar Encoder- In this step, provides the 16 bit input data bits and it converts into the 32 data bits.

Polar Channel- the 32-bit polar encoder output gives in the channel and here it converts into the 288 bits.

Polar Decoder- In this step the channel output gives in the polar decoder and it converts into the 16 data bits.

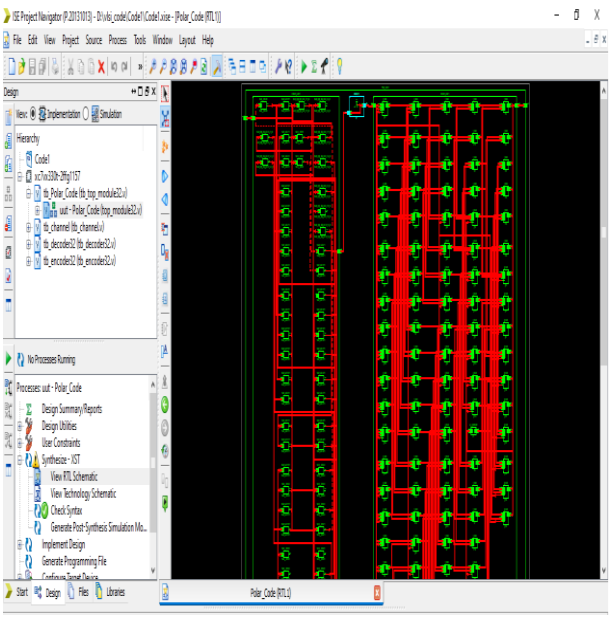

Figure 4: RTL view of proposed model

Figure 4 showing register transfer level diagram which contain all blocks and wires.

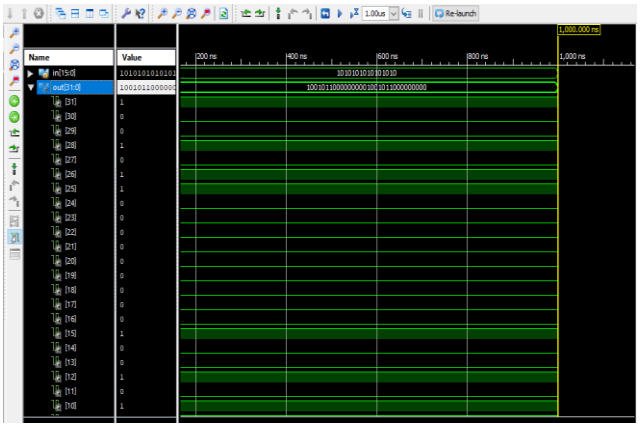

Figure 5: Test bench encoder output waveform

Figure 5 is showing the test bench results. Here the 16-bit input data bits is 1100110011001100 and the data bit is retrieved in the output of the decoder side that is same as input side of the encoder.

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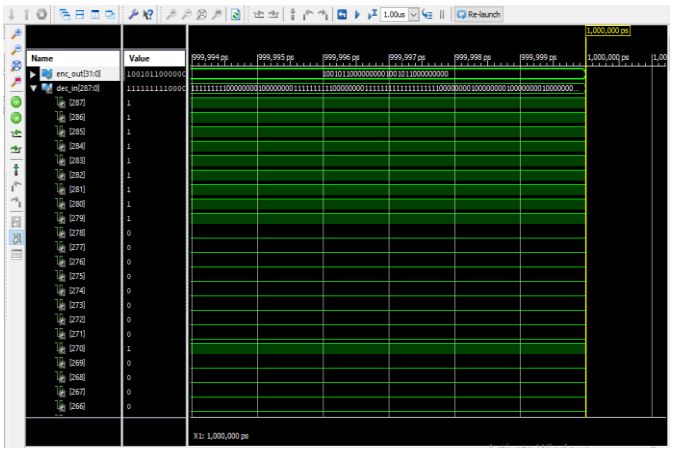

Figure 6: Test bench channel output waveform

Figure 6 showing channel result in test bench, here apply 32 bit encoder output that is 10010110000000001001011000000000.

It generates 288 decoder input bit that is hff80403ff00ffffe0100804020100804020 1ff80403ff00ffffe01008040201008040201 in hexa decimal.

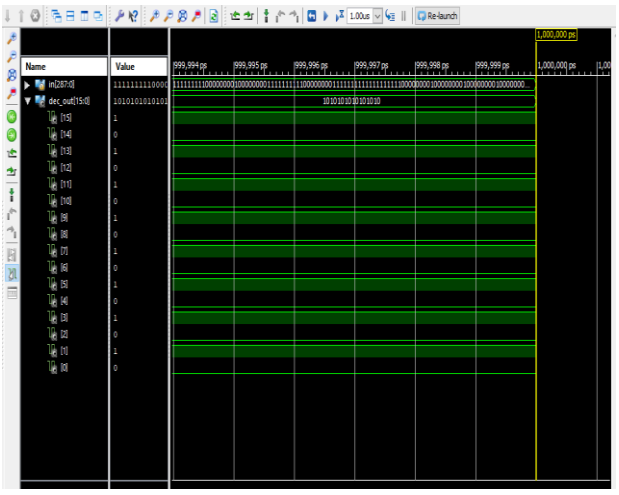

Figure 7: Test bench decoder output waveform

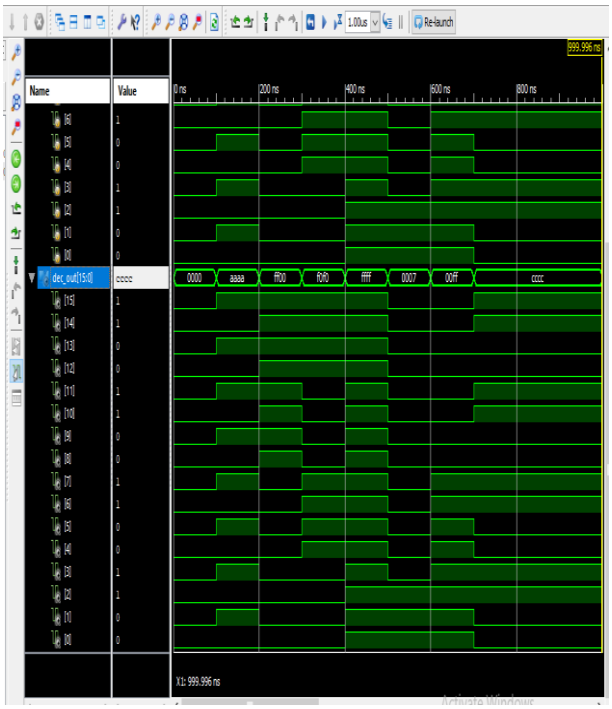

Figure 8: Test bench Result in hexadecimal complete waveform

Figure 8 is showing the various results value in the Xilinx test bench. The input of encoder and output of decoder is the 'cccc' in the form of hexadecimal.

Table 1: Comparison of simulation results

Sr No.	Parameter	Previous Work [1]	Proposed Work
1	Method	Polar Decoder	Polar Encoder & Decoder
2	Area	2.189 mm2	2 mm2
3	Delay	99.94 ns	80.67 ns
4	Power	193.5 mW	125 mW
5	Throughput	11.9 Gbps	12.4 Gbps

V. CONCLUSION

Polar codes have garnered a growing amount of attention in recent years as a result of their minimal encoding and decoding complexity. This paper suggested the FPGA implementation of a polar encoder-decoder for 5G artificial intelligence applications. The total number of components or

area is 2mm2, which is a decrease from the previous value of 2.189mm2. Compared to the previous value of 99.94 ns, the current delay or latency is 80.67 ns. The aggregate throughput is 12.4 Gbps, which is higher than the previous value of 11.9 Gbps. Consequently, the simulation results indicate that the proposed polar code produces significantly superior results than previous work.

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