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Review of VLSI Architecture for Filtering in Computer Vision

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***Abstract*— Image denoising is a critical pre-processing step in computer vision, designed to improve image quality by reducing noise while preserving essential features. This process is essential for enhancing the accuracy of high-level tasks such as object detection, image segmentation, and facial recognition. Traditional software-based denoising techniques struggle to meet the increasing demands for real-time performance in applications like autonomous vehicles, medical imaging, and surveillance systems. Very-Large-Scale Integration (VLSI) architectures provide a hardware-based solution, offering high-speed processing and energy efficiency for image denoising tasks. This review explores the diverse VLSI architectures employed in filtering for image denoising in computer vision, analyzing their computational complexity, power efficiency, and scalability. The paper delves into the benefits and trade-offs of various architectures, including field-programmable gate arrays (FPGAs), digital signal processors (DSPs), and application-specific integrated circuits (ASICs).**

***Keywords*— *Image, Denoising, VLSI, Filter, Noise, FPGA*.**

I. INTRODUCTION

In the field of computer vision, image denoising plays a pivotal role in ensuring the reliability and accuracy of downstream tasks such as object recognition, image segmentation, and feature extraction. The presence of noise, whether introduced during image acquisition or transmission, can severely degrade image quality and impair the performance of vision algorithms. As a result, denoising is a fundamental preprocessing step used to enhance images by eliminating unwanted noise while preserving critical details such as edges, textures, and fine structures.

The increasing demand for real-time image processing in applications such as autonomous driving, medical diagnostics, and security systems has put significant pressure on existing denoising techniques. Software-based methods, while highly flexible and algorithmically advanced, often fail to meet the performance requirements necessary for real-time applications due to their computational overhead and energy consumption. This limitation has led to a growing interest in hardware-based solutions, particularly in Very-Large-Scale Integration (VLSI) architectures, for implementing image denoising filters.

VLSI technology allows for the integration of millions of transistors onto a single chip, enabling the development of custom hardware that can perform complex tasks with high efficiency and low power consumption. By offloading the computational burden from general-purpose processors to specialized hardware, VLSI-based systems can achieve the real-time performance necessary for high-speed computer vision applications. Moreover, these architectures offer the potential for parallelism, which is crucial for handling the massive amounts of data generated in real-time image processing tasks.

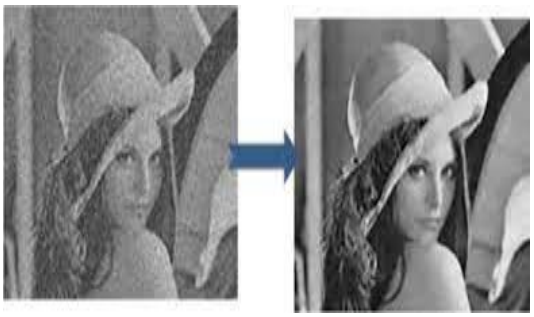

Figure 1: Leena image (a) Noisy (b) Denoised

One of the most common VLSI architectures used for image denoising is the FPGA, which provides reconfigurable hardware that can be tailored to specific filtering algorithms. FPGAs are particularly well-suited for prototyping and real-

time applications due to their flexibility and ability to handle parallel processing. Another popular architecture is the ASIC, which, unlike FPGAs, is a fixed hardware solution designed for a specific application. While ASICs offer superior performance and power efficiency, their lack of reconfigurability limits their use in rapidly evolving fields like computer vision.

In addition to these architectures, digital signal processors (DSPs) have been widely used in image processing tasks. DSPs are designed to handle real-time signal processing, making them ideal for implementing image denoising algorithms. However, compared to FPGAs and ASICs, DSPs may not offer the same level of parallelism, which can limit their performance in highly demanding applications.

Recent advancements in neuromorphic computing and machine learning accelerators are also beginning to influence VLSI design for image denoising. Neuromorphic systems mimic the brain's architecture, allowing for highly parallel, low-power computation, which is particularly useful in noise reduction tasks where preserving fine details is crucial. Similarly, machine learning accelerators, such as Tensor Processing Units (TPUs), are being explored for their ability to enhance denoising performance by leveraging deep learning algorithms to identify and remove noise from images.

II. LITERATURE SURVEY

M. Mody et al.,[1] Bilateral (BL) filtering is becoming de-facto noise filtering for computer vision and analytics processing systems due to its edge-preserving property. The prior literature address - Bilateral filtering by its direct implementation, which has higher computational complexity and is restricted to non-embedded applications. This paper proposes a novel solution to Bilateral filtering with significant complexity reduction enabling 720 MPixel/second throughput hardware IP in 16nm FinFET. The paper proposes multiple novelties namely Space and amplitude quantized Fixed point 2D-LUT, mixed-mode 1D Division LUT, and an efficient content-adaptive algorithm for Bilateral Filtering.

C. Lien et al.,[2] Here, a low-cost apparatus engineering of the appropriate filter for continuous image preparation is presented. The use of multipliers may be cut by 48% as compared to conventional methods, thanks to distance-based collecting and sharing of equipment assets. An efficient quantization method is also used to reduce the quantity of necessary search tables. It has been shown via testing that the suggested design is efficient in terms of both money and time.

M. Monajati et al., [3] They rely on the planning schedule, and they manage to get decent results with cheap equipment. To improve the efficacy of such filters in noise cancellation, it is suggested that a dedicated comparator be developed for this purpose. Our estimated middle filters (IMFs) follow both standard and unique architectures. Showcase the histogram-based error scatter plot as an additional error assessment method for a more thorough examination of IMF implementation. The reproduction results demonstrate that the suggested filter requires negligible investments of time, energy, and resources to implement. While there is a compromise between the filter's precision and its circuit characteristics, its yield nature is very similar to that of an exact filter. Corrupted areas are similarly barely visible to the naked eye.

Using a low-area, highly precise VLSI design, A. Chakraborty et al. [4] suggested a 2D Wiener filter that can be effectively implemented for any1D/2D constant sign. Because of its computational complexity, the Wiener filter, which is inherently very accurate, bogs down. In this piece, we focus on how to overcome this barrier by reducing the computational complexity via the refinement of the Toeplitz framework and the degradation of its QR. a multiplier-free VLSI architecture for recognising 2D Wiener filters has been suggested. have utilised the CORDIC calculation and the concept of Givens turn-based QR degradation to achieve the highest possible level of success with our strategy. have also tried out our suggested apparatus on a continuous basis for signal and image denoising. In contrast to competing layouts, ours stands out in both visual and numerical ways.

The limit cell of MFA is presented to be modified by GS Rajput et al.,[5] who propose a two-phase Query table-based Newton Raphson divider as a replacement for the traditional divider unit. The architecture implemented on Xilinx Virtex-6 FPGA has the highest throughput among state-of-the-art models, denoising 512*512 images at a constant rate of 33

frames per second. The significance of the suggested engineering is shown by a quantitative and subjective evaluation of denoising on synthetic and real images.

This paper by P. Sendamarai et al., [6] presented a two-sided filtering strategy and uses lifting-based DWT for pressure decompression. The XILINX ISE 14.3 test system is used to implement and simulate this concept. To simplify things, a shift-add rationale graphic is shown. When optimised for the Xilinx Austere III seriesfield programmable door cluster, the suggested design is able to function at a frequency of 163.638MHz.

To counteract the error and hasten the delay in the Logarithmic Multiplier's operation, A. Mekkalaki et al., [7] demonstrate the use of a 1616 "Mitchell Log Multiplier" (MLM) based on the "Karastuba Ofman Multiplier." For the sake of error-free photo filtering, this project employs Mitchell Log Multiplier. KOM is used in the design of the more complex 1616 and 88 Multipliers. In order to get the basic square of the request 44 using radix 2, the higher-order KOM multipliers are decomposed into a larger number of lower-order multipliers. The Mitchell Log Multiplier is designed to be completely error-free thanks to its built-in error correction mechanism. In addition, a Gaussian filter based on a "Mitchell Log Multiplier" with a factor of 8 is tested in an effort to remove noise from the image. Xilinx 14.5 is used to simulate the project's model, and the Simple 6 FPGA series is used for integration. The limits of the presentation are evaluated, including presentation velocity, blunder region use, and peak signal to noise ratio. As can be observed, a PSNR of 25.11 DB and a delay of 6.629ns are obtained with the use of the Mitchell log multiplier zero /0 for the duplicating process.

Typical and restricted arranging, then a choice-based yield choice unit, are the two steps of engineering suggested by Kamarujjaman et al. [8]. The notion of choice-based flexible windowing is included into the decision-based yield selection phase to improve incentive commotion hiding and edge conservation. Some recently suggested works have comprehensive quantity and visual quality, and the overall results for proposed engineering are proven to favour its execution above any condition of-craftsmanship technique. Using a Vertex 5 FPGA board, our engineers can process at a speed of 254 MHz. The computations are not very complicated, and there is no need for a line buffer. Cost-wise, it's on par with other low-cost options, and it's especially useful for always-on applications like clinical image processing.

The suggested sharp filter by R. Pushpavalli et al., [9] is carried out in two stages. At the outset, we apply a special type of exchanging middle filter on the corrupted image. In the second step, the filtered output image is sensibly fused with a feed forward neural architecture. By anticipating three important images, the inner borders of the feed forward neural architecture may be adaptively simplified. The elimination of driving noise is accomplished with great success. The simulation results demonstrate the superiority of the proposed filter in eliminating drive noise while preserving the edges and fine details of digital images. The results are compared to other available filters for evaluating the effectiveness of an execution.

An efficient low-cost VLSI architecture for the edge-saving incentive commotion evacuation approach has been presented by P. Deepa et al. [10]. Two line cradles, register banks, a motivation commotion identifier, an edge-located clamour filter, and a drive authority are all part of the engineering. Two-line support, rather than complete edge memory, is required to accommodate the proposed apparatus. In addition, the suggested computation uses a fixed-size window rather than a dynamic one. Both of these measures greatly reduce the need for stockpiling and the complexity of related calculations. If the active pixel is silent, the noise motivation indicator will shut off the surplus hardware. Also, the designing of a four-phase pipeline has a tremendous impact on productivity. Incorporating an edge-protecting computation into the denoising process improves the final image's clarity. Therefore, the suggested design is easier to implement, requires less resources, makes less use of force, and improves performance speed. The engineering was carried out in Xilinx 9.2i, and the results are laid forth for various images.

The suggested procedure by C. Lien et al., [11] may improve upon previous, less complex methods in terms of quantitative evaluation and visual quality. More so, the display may look and feel much like the more advanced, intricate methods. Our

plan's VLSI engineering uses TSMC 0.18 m technology to provide a handling speed of around 200 MHz. When compared to state-of-the-art methods, our technique can reduce memory hoarding by over 90%. The design only requires two-line memory cradles and little computing complexity. Its modest initial investment makes it a good choice for use in applications that need consistency.

The suggested work by K. Vasanth et al., [12] makes use of a different convey select comparator in the primary segment, one that makes use of consider and trade capabilities, and its pipelined form in the secondary segment, simplifying the arranging organisations. Unlike other comparator designs, the one-half subractor and seven-full subractor used in the proposed Convey choose comparator mean less multiplexers and inverters are needed. As the suggested approach completes the critical computation in just 7 clock cycles, it will eliminate the problems. The pipelined variation of the work compared well to the original in terms of space savings, power consumption, and frequency (113.225 MHz) for the Gadgets XC2s100e-7tq144.

III. CHALLENGES

Scalability and Flexibility

As image resolutions increase and applications become more demanding, scalability becomes a critical factor in VLSI design. The architecture needs to handle a wide range of image sizes, from low-resolution images to ultra-high-definition ones, while maintaining consistent performance. Moreover, flexibility is essential for adapting to the rapidly evolving algorithms in computer vision. While ASICs provide high efficiency for specific tasks, they lack the flexibility to adapt to new techniques or upgrades in filtering algorithms, such as advanced neural networks for denoising. Conversely, FPGAs offer flexibility but may not match the performance and power efficiency of ASICs, leading to a trade-off that must be carefully considered.

Complexity of Denoising Algorithms

Image denoising algorithms have evolved to handle complex noise patterns and preserve intricate image details. Advanced algorithms like wavelet-based denoising, non-local means (NLM), and deep learning-based methods introduce significant computational complexity, which is difficult to implement efficiently in VLSI architectures. The challenge is to simplify or approximate these algorithms for hardware implementation without significantly degrading their effectiveness in noise reduction. Achieving this balance between algorithm complexity and hardware feasibility remains a critical issue for researchers.

Real-Time Processing Requirements

Many computer vision applications, such as autonomous driving and surveillance, require real-time processing of video streams. The VLSI architecture must be capable of handling high-throughput data with minimal latency to ensure timely decisions. For example, in autonomous vehicles, delays in processing can have severe consequences. Real-time constraints often limit the complexity of algorithms that can be implemented, forcing designers to find efficient hardware optimizations and parallelization techniques that maintain the necessary speed without compromising accuracy.

Hardware Area Constraints

In VLSI design, space is a precious resource. Increasing the computational power of a chip often requires adding more processing units or more complex circuitry, which increases the physical area required. However, there are strict limitations on the chip area due to cost, yield, and power consumption considerations. Therefore, designers must carefully allocate resources to achieve the desired performance while minimizing the area footprint. This trade-off between area, power, and performance is especially challenging when integrating complex denoising algorithms.

Noise Variability and Adaptability

Noise in images can vary significantly depending on the acquisition process and environmental conditions. For example, noise in medical images differs from that in surveillance footage or satellite imagery. Designing a VLSI architecture that can adapt to different noise types and levels is challenging. Static hardware architectures may not handle dynamic noise conditions well, necessitating more adaptable solutions that can modify their behavior based on the noise characteristics of each image. While reconfigurable architectures like FPGAs offer some adaptability, achieving this in highly efficient fixed architectures like ASICs is more difficult.

IV. CONCLUSION

Using image denoising, may fix distorted or noisy pictures. In addition to a wide variety of uses, such as restoring clarity to blurry photos, the technology also has a wide range of applications. Therefore, picture denoising is useful in several contexts, including those where recovering the original image content is critical for good performance, such as in image restoration, visual tracking, image registration, image segmentation, and image classification. In this study, we take a look at the state of the art in VLSI-based filter approaches for denoising images.

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