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Review of VLSI Architecture of Rationalized Bi-Orthogonal Wavelet Filter Banks

[1]Prachi Sharma, [2]Dr. Monika Kapoor
[1]Research Scholar, [2]Professor
[1,2]Department of Electronics and Communication Engineering
[1,2]Lakshmi Narain College of Technology, Bhopal, India

***Abstract*— Wavelet transforms have become essential tools in signal processing, especially for tasks such as image compression, denoising, and feature extraction. Among the various wavelet families, Bi-Orthogonal Wavelet Filter Banks (BOWFBs) offer the distinct advantage of having both symmetric wavelets and perfect reconstruction, making them ideal for applications requiring high-quality signal recovery. However, implementing BOWFBs efficiently in hardware remains a challenge due to the complexity of the mathematical operations involved. Rationalized Bi-Orthogonal Wavelet Filter Banks (RBWFBs) provide a modified approach that reduces computational complexity while preserving the essential features of BOWFBs. This paper presents a detailed review of VLSI (Very Large Scale Integration) architectures for RBWFBs, focusing on their design strategies, hardware optimizations, and trade-offs.**

Keywords*— *Filterbank, BOWFBs, VLSI, Channel, Delay, Complex, Hearing Aid.

I. INTRODUCTION

Wavelet transforms have revolutionized various fields of signal and image processing by providing a flexible and efficient way to represent signals at multiple levels of detail. Unlike traditional Fourier transforms, which offer only frequency-domain information, wavelets provide both time and frequency localization, making them ideal for analyzing non-stationary signals. This property has made wavelets indispensable for a wide range of applications, from image compression in standards like JPEG2000 to noise reduction and feature extraction in medical imaging and computer vision.

Within the family of wavelet transforms, Bi-Orthogonal Wavelet Filter Banks (BOWFBs) stand out due to their symmetric wavelet functions and the property of perfect reconstruction. In traditional orthogonal wavelets, the scaling and wavelet functions are not symmetric, which can lead to phase distortion in certain applications. Bi-orthogonal wavelets, on the other hand, maintain symmetry in both the analysis and synthesis wavelets, ensuring that signals can be reconstructed without loss or distortion—a crucial feature for applications such as image and video compression, where quality retention is critical.

Despite their advantages, the implementation of bi-orthogonal wavelets in hardware, particularly for real-time applications, poses significant challenges. The mathematical operations required for bi-orthogonal wavelet transforms are computationally intensive, involving convolutions, filtering, and down-sampling. These operations, when applied to high-resolution images or real-time video streams, can overwhelm traditional hardware platforms, especially in low-power environments like embedded systems or mobile devices.

In response to these challenges, Rationalized Bi-Orthogonal Wavelet Filter Banks (RBWFBs) have been proposed as a means of reducing the computational complexity of the standard BOWFBs. The term “rationalized” refers to the simplification of filter coefficients, which reduces the number of operations required for wavelet decomposition and reconstruction. This rationalization makes RBWFBs more suitable for hardware implementations, especially when power, area, and speed are constrained, as in many VLSI applications.

The field of Very Large Scale Integration (VLSI) design has seen significant advancements in optimizing the hardware implementation of wavelet transforms. VLSI architectures are critical for achieving real-time performance in wavelet-based systems, as they allow for the parallelization of operations,

pipelining, and hardware-specific optimizations that can dramatically improve throughput and reduce latency. However, designing efficient VLSI architectures for wavelet transforms, particularly for RBWFBs, requires a deep understanding of both the mathematical underpinnings of wavelets and the constraints of hardware platforms.

The rationalization of bi-orthogonal wavelets simplifies the filter design, but it also introduces trade-offs. While computational complexity is reduced, the fidelity of the wavelet transform may be impacted if the rationalization process overly simplifies the filter coefficients. Therefore, careful consideration must be given to the balance between complexity and signal fidelity in the design of VLSI architectures for RBWFBs. Additionally, hardware constraints such as power consumption, chip area, and processing speed must be factored into the design process, especially in applications like real-time image processing, where performance is critical.

II. LITERATURE SURVEY

A. K. Samantaray et al., [1] presented a novel generalized approach to obtain rational (dyadic and integer) bi-orthogonal wavelet filter coefficients based on two conditions, namely maximally flatness and near-perfect reconstruction (PR) in half-band polynomial (HBP). An incremental-iterative approach is adopted to design the coefficients based on the proposed error equation in terms of the remainder polynomial (RP) of Lagrange HBP and the proposed HBP with maximum vanishing moments (VMs). In addition, VLSI architecture for the proposed wavelet filter banks (FBs) is designed and implemented on the Zedboard ZYNQ-7000 AP-SoC (Zynq FPGA from Xilinx) field-programmable gate array. It is found that the proposed rationalized wavelet FBs achieved significantly low digital hardware requirements with similar characteristics when compared to well-known rationalized existing bi-orthogonal wavelet FBs.

K. Kaustubh Banninthaya et al.,[2] presents a system with reconfigurable warped VDF that uses a single prototype filter for generating all the necessary sub-bands. The proposed system automates the generation of the control signals for reconfiguring the filter and pipelines the processing of each sub-band to generate the requisite magnitude response. The proposed architecture is designed to achieve good audiogram matching with minimum matching error.

S. C. Lai, C. H. Liu et al.,[3] presents a novel algorithm design of 18-band quasi-class-2 ANSI S1.11 1/3 octave filter bank with the advantages of low group delay and low complexity. The proposed method utilizes a simple low-pass filter (LPF) and discrete cosine transform (DCT) modulation to generate a uniform 9-band filter bank first, and then transfer all element of z-1 into all-pass filter in order to obtain the non-uniform filter bank to meet the standard. Quasi-class-2 ANSI S1.11 design, the proposed method totally has 63.4% reduction for multiplications per sample and 14-ms group delay, although we still have 15.2% increase for additions per sample.

A. Vijayakumar et al.,[4] shows that the design criteria of p th order analysis having q th order synthesis filters ($p \neq q$) with a flexibility to control the system delay has never been addressed concomitantly. In this paper, we propose a systematic design for a filterbank that can have arbitrary delay with a (p, q) order. Such filterbanks play an important role especially in applications where low delay-high quality signals are required, like a digital hearing aid.

Y. Wei et al.,[5]. the proposed filterbank can achieve a better matching to the audiogram and has smaller complexity compared with the fixed filterbank. The drawback of the proposed method is that the throughput delay is relatively long (>20 ms), which needs to be further reduced before it can be used in a real hearing-aid application.

A. Schasse, et al.,[6] present an efficient method to increase the frequency resolution for speech enhancement algorithms in hearing aids. Since the analysis-synthesis filter-bank applied in digital hearing aids needs to deliver a high stop band attenuation to enable large frequency dependent amplification gains and a low overall delay, speech enhancement often suffers from the resulting low frequency resolution. This leads to residual noise artifacts in the processed speech, since the noise between the harmonics can not be removed.

R. Dong et al.,[7] To help develop ultra-low power wireless hearing aid products, we investigate the integration of subband

audio coding with hearing aid applications. Both the audio coding and the hearing aid application use subband processing, but their requirements for the filterbanks are totally different. A joint filterbank structure is proposed in this paper to satisfy these contradictive filterbank requirements. With this structure, the two filterbanks are combined into a single stereo filterbank operation, which can be efficiently implemented on a filterbank coprocessor. This structure substantially reduces the computation complexity, power consumption and memory usage.

R. Vicen-Bueno et al.,[8] presents the categories, the added stable gain (ASG) value over the limit gain of the digital hearing aids is obtained. The ASG value is achieved as a tradeoff between the segmented signal-to-noise ratio (objective parameter) and the speech quality (subjective parameter). The results show how the digital hearing aid working with a feedback reduction adaptive filter adapted with the NFXLMS algorithm is able to achieve up to 18 dB of increase over the limit gain.

R. Vicen-Bueno, R. Gil-Pita et al.,[9] presents the description of a hearing aid simulation tool. This tool simulates the real behavior of digital DSP-based hearing aids with the aim of getting a very promising performance, which can be used for further design and research, and for a better fitting of the hearing-impaired patient. Results using a multilevel multifrequency hearing aid with real data collected from 18 patients show how the multifrequency compression techniques adapt the normal perceptible sounds to the hearing-impaired patient perceiving area.

B. Swanson et al.,[10] The Nucleus Freedom cochlear implant system enables a profoundly deaf person to hear. The system consists of a surgically implanted stimulator and a battery-powered external sound processor. The processor is based on a 0.18 μm CMOS ASIC containing four DSP cores. The signal processing includes a two-microphone adaptive beamformer, a 22-channel quadrature FFT filterbank, multi-band automatic gain control, a psycho-acoustic masking model and non-linear compression. The key design challenge was power consumption.

III. HEARING AID APPLICATION & CHALLENGES

For hearing aid use, the frequency splitting is performed for the purpose of modifying the spectral shape of the input signal. Hearing aid fitting typically requires a wide gain adjustment range. In a compression system, the input signal level, which can be measured as the overall level, channel level or a combination, controls these gains.

The spectral shape of the input signal is modified at this point by applying suitable gains to the frequency channel signals. This is followed by the corresponding inverse odd (even) FFT, interpolation, synthesis window weighting and the overlap-add procedure. This window (a low-pass filter which is the counterpart to the analysis window), minimizes the spectral imaging distortion created during the interpolation step.

Given the requirement for wide gain adjustment, the alias cancellation theory is invalid and critical sampling is insufficient. This problem necessitated the development of an oversampled filterbank. Although oversampling increases the data rate, it is the price that must be paid for gain adjustability without aliasing. In a compression system, gain changes are dynamic. This may cause anomalies in the overall frequency response if phase differences exist between adjacent bands.

To avoid these undesirable frequency response notches or peaks at the band edges (which frequently occur in analog systems), it is necessary to constrain the filter channel impulse responses to be linear phase and of equal delay.

Thus, an ideal filterbank for a hearing aid application would:

- Allow precise fitting of prescriptive targets
- Have short delay
- Be computationally efficient
- Use a minimal amount of memory.

IV. CONCLUSION

This paper studies about the various researches on the digital filter bank for the hearing aid applications. Several tradeoffs have been made to make filterbank that can meet the requirements of a hearing aid application. The filterbank

structure is M-band with uniform bands. This type of structure provides many advantages in a hearing aid context. To conserve memory, only a single analysis window is stored. To further reduce memory, the synthesis window is created by decimating the analysis window, subject to time and frequency domain constraints that can be satisfied by using an filter design method.

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