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CMOS Reversible Realization 8-bit Add-Sub Circuit with Optimized Quantum Cost

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***Abstract*: - The Full Adder serves as a fundamental element within any central processing unit, being an essential component utilized across all processors. In efforts to reduce power loss in digital devices, researchers have turned their attention to reversible logic. This paper provides an analysis of area delay concerning a CMOS reversible gate-based add-sub circuit intended for VLSI applications. The proposed design is evaluated against existing designs based on selected performance metrics, including the total count of reversible gates, garbage outputs, and quantum cost. An 8-bit adder-subtractor circuit employing a reversible logic approach was simulated using the Modelsim tool and synthesized for Xilinx ISE 14.7.**

Keywords: - Adder, Xilinx, Reversible Realization, components, Gates, Garbage Output.

I. INTRODUCTION

Reversible logic operations are characterized by their inability to erase information and their capacity to dissipate no heat. These circuits function in reverse, enabling the reconstruction of inputs from outputs while consuming no power. Logic gates, as fundamental components of any logic circuit, are employed to implement Boolean functions. A Reversible Logic Gate must establish a one-to-one correspondence between inputs and outputs to ensure reversibility. This means that a Reversible Gate is bijective with respect to inputs and outputs. It not only facilitates the determination of outputs from inputs but also allows for the unique recovery of inputs from outputs. When necessary, additional inputs or outputs can be introduced to achieve a balance between the quantities of inputs and outputs. This also pertains to the outputs that are not utilized in the synthesis of a specific function. In some instances, these additional elements are essential for ensuring reversibility. The equation can be expressed as Inputs + Constant Inputs = Outputs + Unused Outputs. Fig. 1 illustrates an n-input and n-output Reversible Logic Gate, referred to as an n*n Reversible Logic Gate, where the nth input is designated as in and the nth output is labeled as on.

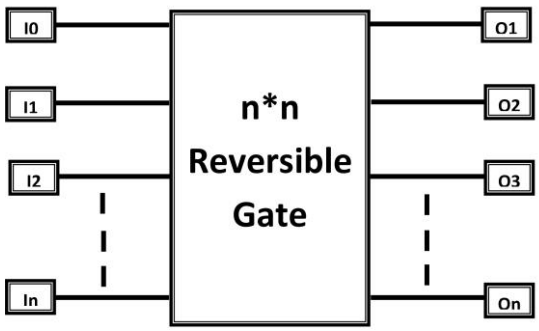

Figure 1: n*n Reversible Logic Gate

Numerous reversible gates are documented in the literature. Notably, the 2x2 WG Gate in Fig.2 and the 3x3 WG Double Gate is among the most favored options.

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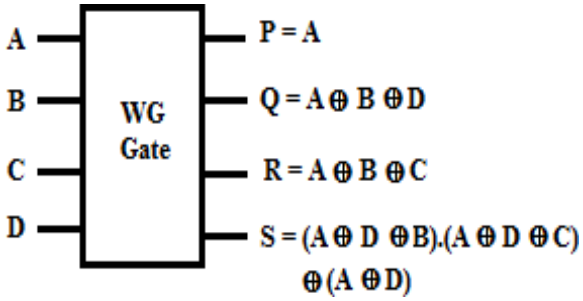

Figure 2: WG Gate

Garbage Outputs

These are defined as the unused output signals generated from the designed reversible digital circuit. Garbage output signals generate power loss from the designed eversible circuits.

Ideally zero garbage output signals should be generated from the designed circuit. Garbage output signals deteriorate the performance of the designed reversible circuits, so researchers focus to minimize them with the aim to obtain an efficient reversible electronic device.

1.1 Quantum Cost

Quantum cost of any reversible logic gate or circuit is defined as the total number of 1×1 or 2×2 size basic reversible logic gates required to design the given reversible logic gate or device. Here quantum cost of 1×1 size basic reversible gate is zero, whereas quantum cost of 2×2 size basic reversible gate is one. So summation of total quantum cost of these basic gates provides the cost of overall circuit. Quantum cost of any reversible circuit affect the performance of the designed reversible circuit. So researchers emphasize on the minimization of the quantum cost of the reversible circuit to improve the performance of the designed reversible circuit.

1.2 Reversible Circuit Design

Reversible approach redesigns digital circuits with the help of reversible logic gates only. Here the main aim is to minimize the bit loss to generate ideally lossless digital circuits. Some required characteristics of designed reversible digital circuits are as follows:

- Minimum number of reversible logic gates used to design the target digital circuits.
- Minimum number of garbage outputs.
- No feedback connection.
- Low quantum cost.

Based on above characteristics researchers have already designed various digital circuits with reversible approach. Further improvements in the designs are being proposed by researchers for better efficiency with optimized performance parameters.

II. METHODOLOGY

The 8-bit adder/subtractor is designed to calculate the sum or difference of two 8-bit numbers, designated as A and B. This operation employs an 8-bit carry look-ahead adder in conjunction with either 2's complement or a multiplexer to facilitate subtraction.

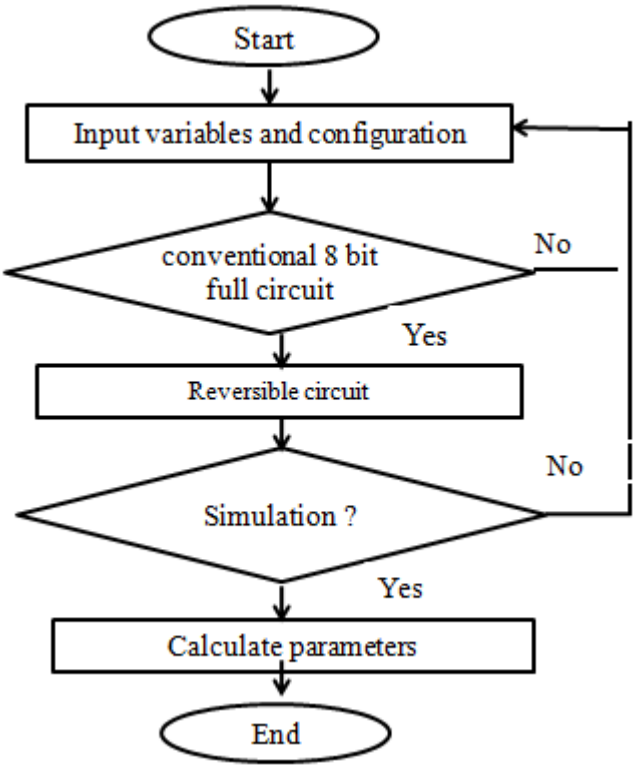

Figure 3: Flow Chart

When the enable bit is set to low, the multiplexer allows input B to pass through, resulting in the computation of A+B. Conversely, when the enable bit is set to high, the multiplexer transmits the output of the complement, enabling the adder to compute A plus the 2's complement of B, effectively yielding A-B. In the case of adding the numbers 10100010 and 11100011 (with the enable set to low), the maximum delay for the multiplexer in the schematic is 0.02975 ns. This delay must be combined with the clock delay

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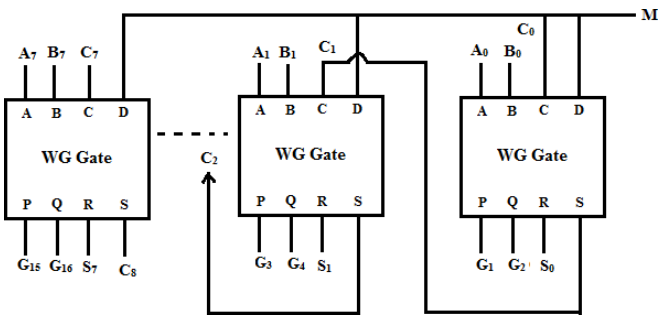
of the 8-bit adder, resulting in a total clock delay of 0.02975 ns + 0.110126 ns = 0.139876 ns. Therefore, the earliest point at which the schematic clock can



transition for addition is 0.14 ns following the setting of the inputs.

The delay associated with the layout was measured at 0.12012 ns. When this value is combined with the delay from the 8-bit adder, the total clock delay amounts to 0.12012 ns + 0.259166 ns, resulting in a cumulative delay of 0.379286 ns. Consequently, the earliest moment at which the extracted clock can transition for addition are 0.38 ns following the setting of the inputs, above reversible logic gates are used to design different combinational as well as sequential digital circuits with reversible logic approach.

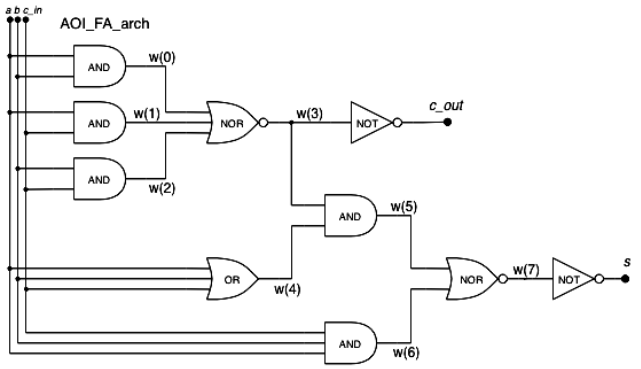


Figure 4: Full adder

The primary component that requires attention is the Full Adder, which serves the purpose of determining the sum and carry when adding two 1-bit numbers. Although there are various methods to construct a full adder, the project utilized the AND-OR-Invert (AOI) configuration as depicted in Fig.4. This component consists of three 1-bit inputs and two 1-bit outputs: a and b (the numbers being added), c_in (the carry in), c_out (the carry out), and s (the sum of a+b+c_in).

Prior to proceeding further, it is essential to clearly define the terms carry and entirety, which can be most effectively accomplished through an example. Consider the addition of the decimal numbers 5 and 6. When adding these numbers, if we try to represent the number "11" in the ones place, we must carry a 1 to the tens place, resulting in a total of 1 in the ones place. A similar process occurs in binary addition. When adding 1 and 1 in binary, we cannot represent "2" in the ones place, so we carry a 1 to the twos place, resulting in a total of 0. This concept is applicable to the full adder. The sum (s) represents the remainder of the total a+b+c_in, after a carry (c_out) has been generated, if necessary. Therefore, the purpose of the full adder is to determine the sum of two 1-bit numbers and a 1-bit carry-in.

Figure 5: Reversible Realization of 8-bit Adder-Subtractor circuit

As shown in figure 5 below, this design approach employs WG gate as the adder-subtractor unit. Here eight WG gates are cascaded to design the target 8-bit adder-subtractor circuit using reversible logic approach. Binary numbers A and B are applied to the first two inputs of WG gates, whereas, third and fourth inputs of WG gates are connected to carry and mode bit. Here only eight WG gates are used to design the target adder-subtractor circuit.

III. SIMULATION RESULTS

The proposed algorithm has been implemented and simulated using Xilinx 14. For the simulation process, the behavioral modeling style and Isim simulator have been utilized. Additionally, results pertaining to RTL and synthesis have been produced.

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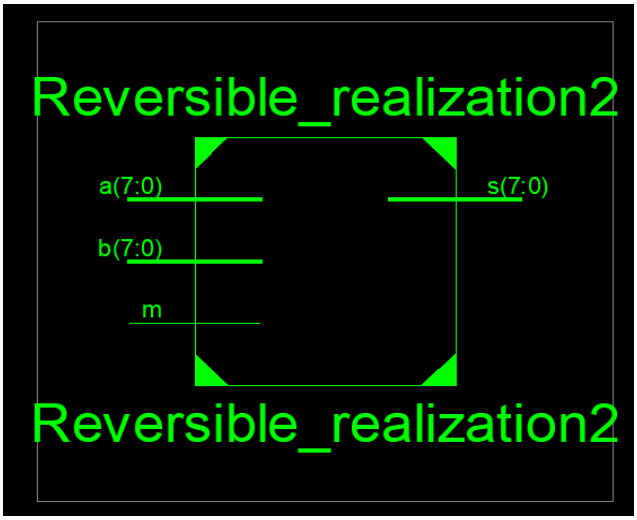

Figure 6: Proposed Top module

Figure 8: Result in test bench Conventional 8 bit full adder/Subtractor

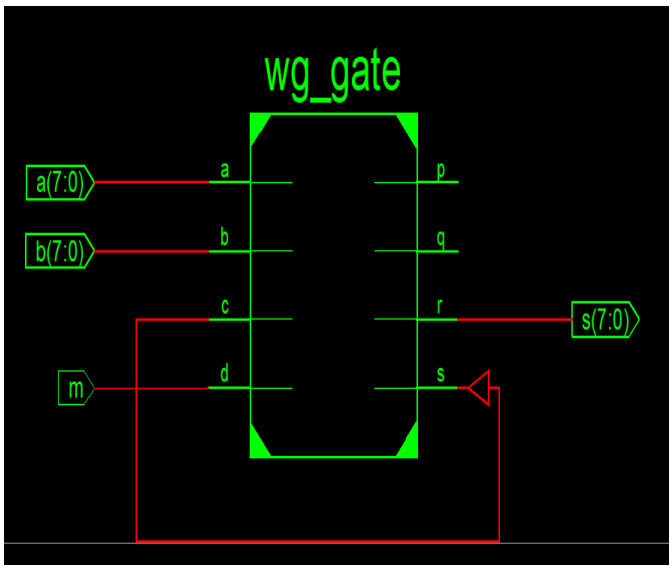

Figure 7: Proposed Reversible circuit using wg_gate

Fig.7 illustrates a reversible circuit that employs wg_gate, with the WG gate being the sole component successfully implemented in NMR nanotechnology. The quantum cost associated with the WG gate is quantified as 10. Furthermore, it has been noted that WG gate exhibits superior performance compared to TSG, MKG, and HNG regarding hardware complexity. The configuration consists of four WG gates and necessitates four constant inputs. The quantum realization cost for the proposed design amounts to 40, resulting in the generation of 14 garbage outputs.

Table 1: Result Comparison

Sr no.	Parameter	Previous work [1]	Proposed work
1	Number of Gates	16	10
2	Garbage Output	17	14
3	Quantum Cost	72	40

The optimization is realized through the careful selection of specific factors, including the number of gates, the amount of garbage outputs, and the quantum cost in relation to current designs. The proposed adder-subtractor circuit is constructed using merely 10 gates, produces 14 garbage outputs, and has a total quantum cost of 40. This circuit can be employed in a range of computational devices aimed at creating low-power loss electronic systems.

IV. CONCLUSION

The final entity was subjected to testing through the selection of cases that would illustrate the successful addition and subtraction functionalities of the 8-bit adder/subtractor, while also identifying values that result in meaningless outputs. The constraints imposed by the design were clearly outlined. By comparing the output timing diagrams in ModelSim with a truth table derived from arithmetic calculations, the correctness of our Verilog code in faithfully representing the 8-bit adder/subtractor network was ultimately validated.

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