International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347 - 6435 (Online) Volume 13, Issue 9, September 2024)

Analysis of Reversible Realization Adder Subtractor Circuit

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***Abstract*— Reversible logic computation stands out as a crucial and highly promising technology utilized in the creation of low-power digital circuits, optical information processing, quantum dot cellular automata, fault-tolerant systems, and nanotechnology. Traditional digital circuits tend to consume a considerable amount of energy due to the deletion of multiple bits of information during operations. However, in reversible computation, the information bits remain intact. This research paper delves into the exploration of implementing a reversible version of the adder-subtractor circuit.**

Keywords*— *Digital, Reversible, Realization, Adder, Subtractor.

I. INTRODUCTION

Reversible computing has garnered significant attention as a cutting-edge technology with potential benefits in low-power design, quantum computing, and various other fields. The current approach to functional synthesis for reversible circuits involves two main stages. Initially, an embedding step is carried out to differentiate nonunique output patterns by introducing additional variables. Subsequently, the function undergoes synthesis to produce a reversible circuit. However, the sequential treatment of embedding and synthesis poses notable challenges. The embedding process may not always align with the requirements of the subsequent synthesis phase, leading to inefficiencies. Moreover, the introduction of extra variables during embedding can result in a substantial increase in the function's complexity, particularly in the worst-case scenario. This approach may hinder the overall efficiency and effectiveness of the reversible circuit design process.Quantum processing relies heavily on the concept of reversibility, as the progression of a quantum framework is represented by a unitary operator, making it reversible. Quantum cost is also a crucial factor in reversible circuits, with the lowest quantum cost indicating the least expensive reversible circuit. Achieving the lowest quantum cost is essential for the development of a quantum computer. This paper aims to demonstrate how to identify the lowest quantum cost and introduces an advanced Toffoli Gate with the least quantum cost. Quantum cost, which refers to the overall expenses associated with the use of Reversible Logic Gates in designing a circuit, is determined by calculating the actual cost of the raw gates required for implementing Arithmetic and Logic circuit units. Some research introduces a 3*3 reversible gate known as the Advanced Toffoli gate, featuring 3-input lines and 3-output lines. The key attractive feature of this gate is its low quantum cost, with a quantum cost of 3, which is less than the 5 quantum cost. It operates under specific conditions and may have the same applications as the traditional Toffoli gate.

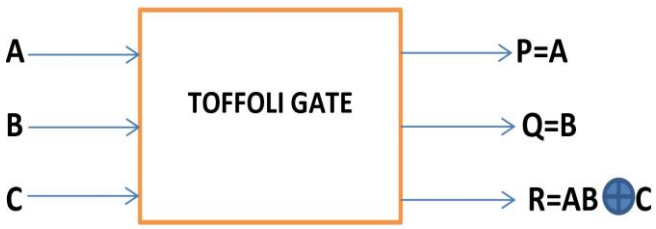

Figure 1: Toffoli Gate

Recently, experts have been focusing on low power efficient digital devices. This particular topic has intrigued researchers to delve into the reversible digital circuit design method. Under ideal conditions, reversible circuits result in zero power loss while enhancing performance. The reversible circuit design method is being increasingly utilized in the fields of DNA computing, low power CMOS design, nanotechnology, quantum computing, optical computing, and more.

II. LITERATURE SURVEY

S. Majumder et al., [1] discuss the growing demand for circuits with low power consumption and reduced computation time in the field of VLSI technology. The authors emphasize the significance of reversible logic in meeting these requirements, highlighting the applications of various reversible gates such as the Feynman Gate, Peres Gate, Modified Fredkin Gate, Modified Toffoli Gate, and TS Gate. This paper provides a comprehensive evaluation of these gates, including their transistor implementation, simulation results, and measurements of average power consumption and delay. Additionally, the study explores the use of TSG in constructing a fully reversible full adder, demonstrating the potential of these implementations in low-power, high-speed circuits suitable for silicon integration

M. T. Emam et. al., [2] This study introduces two innovative designs for Adder/Subtractor using reversible logic gates. The first design is a implementation of two's complement Adder/Subtractor suitable for signed/unsigned numbers. The second design introduces a novel reversible gate that can function independently as a reversible Full Adder/Subtractor unit. The proposed Full Adder/Subtractor is then utilized to design a reversible 4-bit ripple Adder/Subtractor. Reversible logic gates are increasingly sought after for future computing technologies. Reversible logic is emerging as a significant research area with applications in various fields such as low power CMOS design. The paper presents the design of a full Adder/Subtractor circuit using fault tolerant reversible logic gates. This design can operate independently as a reversible Full Adder/Subtractor unit. The proposed design features an equality preserving reversible adder cell, where the equality of the inputs matches the equality of the outputs. This equality preserving reversible adder can be employed to implement any arbitrary Boolean function. It allows for easy detection of any fault affecting only a single signal at the circuit's primary outputs. The proposed structure offers reduced hardware complexity and is efficient in terms of gate count, garbage outputs, and constant inputs compared to existing counterparts.

M. Kumngern et. al., [3] This study introduces a novel voltage adder/subtractor circuit that is programmable. The circuit design is based on differential difference current conveyors and MOS switches, offering advantages over traditional adders and subtractors due to its lower active components, reduced power consumption, and the ability to be programmed using digital codes, making it suitable for integrated circuit applications. Simulation results obtained using the PSPICE program are also presented. The simulation results indicate that the proposed adder/subtractor has an operational range of ±1.5 V with a supply voltage of ±2V and can operate at frequencies up to 100 MHz.

J. Kuppusamy et. al., [4] the testing phase accounts for a significant portion of the overall cost of assembling digital circuits. A reduction in the number of tests conducted can lead to a decrease in both the assembly cost and the market cost of digital circuits. The primary objective of this research is to minimize the number of tests required to detect faults in combinational circuits. The authors have proposed a new method consisting of three stages. The first stage identifies independent faults, while the second stage generates tests for the faults identified in the first stage. The third stage aims to minimize the number of tests generated in the second stage using the Zero One Linear Programming (ZOLP) system. The problem is formulated using the duality theory of linear programming, where independent fault set identification is represented as dual and test minimization is represented as primal. The solution to the dual problem yields a Constrained Independent Fault Set (CIFS), while the solution to the primal problem limits the generation of all possible test vectors. Two-output adder/subtractor circuits, comprising AND, OR, and NOT gates, are utilized as the experimental setup for this purpose.

S. Sultana et. al., [5] This work introduces a new approach to implementing a reversible square-root circuit with a cluster structure. The square root operation is crucial in logical calculations, numerical analysis, computer graphics, and complex number computations. While traditional

irreversible circuits have been used for square root calculations, the emergence of reversible circuits as an alternative has led to the development of a novel reversible implementation for this task. The proposed design includes a reversible controlled adder/subtractor (RCAS) square based on 2's complement arithmetic, serving as a fundamental module. Multiple RCAS squares are utilized in the design, performing addition or subtraction based on the results obtained from digit-by-digit square root operations. This systematic approach represents a significant advancement in the implementation of reversible square root circuits. The circuit's new structure and various parameters, such as the number of gates, garbage bits, and quantum cost for n-bit computation, are detailed in this study. This comprehensive analysis provides insights into the efficiency and performance of the proposed reversible square-root circuit, showcasing its potential for various applications in computational tasks.

K. Jagannatha et. al., [6] over the past few decades, reversible logic has emerged as a highly promising research area and has been applied in various technologies such as low power CMOS, nano-computing, and optical computing. Reversible logic gates are widely recognized for their compatibility with future computing technologies that dissipate minimal heat. Adders play a critical role in many computational systems, and as a result, several adder circuits have been replicated using reversible gates. This study presents a design of an Adder/Subtractor using reversible logic gates. The primary design is an implementation of a two's complement Adder/Subtractor suitable for signed/unsigned numbers. The Full Adder/Subtractor is then utilized to create a reversible 4-bit ripple Adder/Subtractor. It has been demonstrated in Rhythm's tools that reversible circuits outperform irreversible circuits in terms of delay and power distribution.

H. Thapliyal et. al., [7] Reversible circuits have the capability to generate a unique output vector for each input vector, and vice versa, establishing a coordinated mapping between the input and output vectors. The paper's contributions include a novel reversible gate designed specifically for reversible arithmetic, various structures for reversible arithmetic such as binary and BCD adders, subtractors, and comparators, as well as numerous reversible sequential circuits including locks, flip-flops, and shift registers. Unlike previous works, the aforementioned designs are optimized for various parameters such as ancilla and garbage bits, quantum cost, and delay. Another significant contribution is the use of efficient reversible logic for online and offline testing of single and multiple faults in both reversible and conventional logic VLSI circuits.

A. Sarker et. al., [8] Reversible computing has garnered significant attention in recent years due to its increasing application in various fields. This study introduces a new approach to combining addition and subtraction operations using fault-tolerant reversible gates with fault detection capabilities. Adders and subtractors are essential components of any Arithmetic Logic Unit, so the concept of merging these circuits into a single logical block is first presented. Various methods are then discussed to develop fault-tolerant combined addition-subtraction circuits that not only reduce the number of gates but also minimize quantum cost and circuit garbage at a significant level. The study showcases three types of half-adder/subtractor circuits and four types of full-adder/subtractor circuits. Additionally, an algorithm based on the novel concept is described, along with simulations of the proposed circuits. Comparative analysis reveals that the proposed circuit outperforms existing ones, with improvements of 33.33% in garbage output, 26.66% in quantum cost, and a 50% reduction in gate count. Finally, the significance of the proposed designs is emphasized in the conclusion, highlighting the advancements made in fault-tolerant reversible logic circuits for combined addition and subtraction operations.

S. Mukherjee et. al., [9] The fusion of CMOS logic and single electron transistor has revolutionized our current perspectives on nanotechnology. The combination allows for ultra low power consumption and the creation of ultra-thick circuits, made possible through the collaborative efforts of these two technologies. Future researchers are captivated by the benefits of this hybrid SET-CMOS technology for the development of low power VLSI designs on a nano-scale level. A 4-bit adder/subtractor circuit that operates at room temperature has been designed using hybrid SET-CMOS logic, showcasing significantly low power consumption. The power-delay product has been calculated both numerically and graphically, with XOR gates serving as controlled inverters for selecting between addition and subtraction operations. All simulations have been conducted in SPICE environment, utilizing two separate model files for SET behavior (MIB model) and PMOS operation (BSIM4.6.1). It is evident that the hybrid

structure outperforms the traditional MOSFET structure in terms of performance, making it a promising avenue for future advancements in nanoelectronics.

A. Rahman et. al., [10] The IEEE 754 standard double precision (64-bit) floating point arithmetic unit is crucial in intricate digital signal processing applications. The primary operations, floating point addition and subtraction, need to be optimized to efficiently compute floating point multiplier, divider, and square root. However, the main challenge lies in designing the floating point arithmetic unit hardware that consumes fewer resources of FPGA and ASIC while maintaining a maximum operating frequency with a reduced number of clock cycles. This study introduces a novel, efficient hardware design approach for implementing double precision floating point addition and subtraction. The pipelined hardware design is implemented on Virtex-6 and Virtex-5 Xilinx FPGA. Based on the integration outcome, the maximum operating frequency achieved for the proposed hardware design with a clock latency of 8 cycles is significantly higher than previous hardware designs. Additionally, the area overhead is 50 percent lower compared to earlier proposed hardware designs for computing IEEE 754 compliant double precision floating point addition and subtraction.

A. K. Chowdhury et. al., [11] recently, there has been a growing interest in reversible computation within the realm of low-power circuit design. This study introduces an irreversible IG-A gate, which is then utilized to create an irreversible full adder/subtractor (IAS). The IAS block is further employed to construct n-bit adders and subtractors. The proposed IAS design is thoroughly evaluated and compared with existing reversible techniques. Various aspects such as hardware cost, logic computation, and gate count are carefully examined to showcase the efficiency of the proposed design. The transistor-level implementation and simulation of the IG-A circuit are demonstrated using Rhythm OrCAD Light. The simulation results for the one-bit IAS are validated through Altera Quartus II and ModelSim software. The results of the simulations indicate that the circuit offers reduced hardware complexity when compared to current reversible full adder designs. This research contributes to the ongoing exploration of reversible computation and its potential applications in low-power circuitry

N. J. Lisa et. al., [12] Within this study, a sophisticated design for the quantum ternary adder/subtractor circuit is presented, introducing the concept of the quantum Ternary Peres Gate (TPG). The proposed structure of the quantum ternary adder/subtractor circuit consists of two main components. Firstly, it encompasses the design of a quantum ternary full-adder circuit utilizing the suggested TPG gates. Additionally, it incorporates the proposed adder/subtractor circuit by utilizing the constructed full-adder and M-S gates. Furthermore, a heuristic approach is proposed to design a minimal ternary adder/subtractor circuit. The circuits developed in this study exhibit significantly enhanced performance compared to existing alternatives.

III. CONVENTIONAL FULL ADDER CIRCUIT

The 1-bit adder/subtractor, also known as one bit_add_subtract, is represented as a combination of XOR_GATE and AOI_FA elements in Figure 2. The standard representation involves using components that have already been created by creating instances of the component and then connecting (integrating) the ports of each individual instance to the external ports of the element or to internal wires to propagate the signal to other instances.

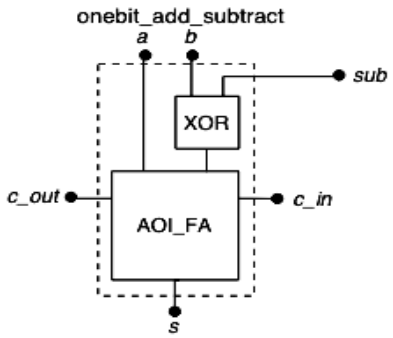

Figure 2: 1-bit adder/subtractor

Table 1 displays that if one input of an XOR gate, such as A, has a value of '0', then the gate functions as a buffer for the other input, resulting in the output being equal to the value of B. If instead A has a value of '1', the gate acts as an inverter, and the output is the complement of B. When the XOR is connected to the second input of the full adder, the input sub can act as a control that determines whether the circuit should add or subtract A and B. If sub is '0', the

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output of the XOR and the input to AOI_FA is simply B, resulting in an adder.

The process of performing double subtraction, such as X-Y, involves a method that incorporates negative numbers using parallel. One approach to achieve this is by employing 2's complement, which is executed by a 1-bit adder/subtractor. The 2's complement essentially converts a positive number in binary to its negative counterpart of equal magnitude, allowing for normal addition. Instead of directly calculating X-Y, the operation is transformed into X+(-Y), where -Y represents the 2's complement of Y. To determine the 2's complement, each digit of Y needs to be inverted to obtain the 1's complement, followed by adding 1 to this result. In the 1-bit adder/subtractor circuit, subtraction occurs when the sub input is '1', causing the XOR output to be the one's complement of B. When the circuit functions as a subtractor, the c_in input must be set to one, enabling the full adder to sum +1 (the two's complement of B) and A.

Table 1: Input output

Case:	sub (c_in)	a	b	c_out	s
1	0	0	0	0	0
2	0	0	1	0	1
3	0	1	0	0	1
4	0	1	1	1	0
5	1	0	0	1	0
6	1	0	1	0	1
7	1	1	0	1	1
8	1	1	1	1	0

The AOI_FA entity was written using dataflow, joining inputs with Boolean operators such as “and”, “or” and “not.” There is more than one way to construct the AOI_FA using VHDL dataflow descriptions. This project described each gate individually, connecting the output of one gate to the input of another using a wire. Alternately the outputs *c_out* and *s* could have been described as a combination of operators in a longer concurrent statement, reducing the number of internal wires needed. This project chose to represent each gate individually to reduce possibility for error when writing a single long concurrent statement. The entity AOI_FA is shown in Figure 3.

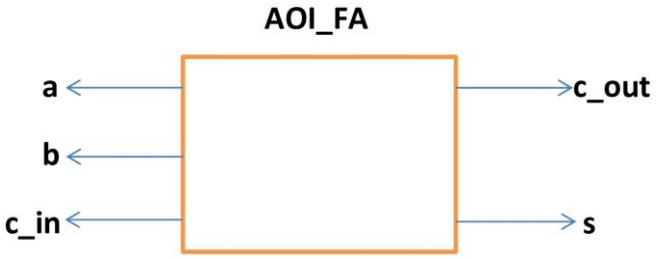

Figure 3: AOI_FA

Following the creation of the AOI_FA illustrated in Figure 4 through VHDL programming, it becomes imperative to verify its functionality. Given that the entity comprises three inputs, there exist a total of 23 distinct combinations of inputs that necessitate testing.

IV. CONCLUSION

Over the last few decades, reversible logic has emerged as a highly promising area of research, with applications in various technologies such as low power CMOS, nano-computing, and optical computing. Reversible logic gates are widely recognized for their compatibility with future computing technologies, as they have the potential to dissipate virtually zero heat. This paper provides a review of the reversible implementation of adder-subtractor circuits, focusing on the use of the dataflow method to describe the lowest level entities, XOR_GATE and AOI_FA. These entities were then combined using the structural description method to create a 1-bit adder/subtractor, which was subsequently scaled up to produce an 8-bit adder/subtractor.

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