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VLSI Architecture of Filterbank with Low Delay for Hearing Aids Application

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***Abstract*— Digital filterbanks in portable hearing assistants utilize a variety of channels to specifically intensify sound of various frequencies to remunerate hearing misfortune. The utilization of filterbanks prompts a higher use of silicon region as there are many channels, each creating a sub-band. Reconfigurable twisted computerized channel is a Variable Advanced Channel (VDF) that can be reconfigured to work as a low-pass, band-pass or high-pass channel with cutoff frequencies. For advanced amplifiers, the channel bank channel should be flexible over a huge unique reach to make up for the meeting misfortune. Different successful channel bank plans with various constructions for advanced portable hearing assistants' applications. This paper presents low delay and low-complexity FPGA digital filter-bank for hearing aids. The simulation shows the significant performance improvement.**

Keywords*— *Digital, filter bandk, delay, hearning aids, VDF, xilinx, MATLAB.

I. INTRODUCTION

Hearing aids are critical devices that enhance the quality of life for individuals with hearing impairments by amplifying and processing sound to meet the user's specific auditory needs. Modern hearing aids are highly sophisticated, requiring advanced signal processing techniques to deliver high-quality sound with minimal delay. Among the key components of these devices are filterbanks, which play a crucial role in breaking down complex audio signals into multiple frequency bands. This enables selective amplification and processing of specific frequencies, improving the intelligibility of speech and other essential sounds. To meet the stringent requirements of real-time performance, power efficiency, and compact design, the development of Very Large-Scale Integration (VLSI) architecture for filterbanks has emerged as a vital area of research and innovation.

A major challenge in hearing aid design is ensuring low delay in signal processing. Delay is a critical metric in hearing aids because any significant lag between the natural and processed sounds can cause disorientation for the user. For instance, delays exceeding 10 milliseconds can lead to a noticeable echo effect, degrading the user experience. The need for low-delay operation necessitates the use of optimized algorithms and hardware architectures that process signals at high speeds while maintaining the integrity and quality of the sound. VLSI technology offers a promising solution by providing hardware-level parallelism and efficiency, which are essential for reducing delay without increasing power consumption.

Filterbanks are the cornerstone of hearing aid signal processing, as they allow sound signals to be divided into smaller, manageable frequency bands. These sub-bands can then be amplified or attenuated based on the user's hearing profile. This frequency-selective approach not only improves hearing clarity but also suppresses background noise, ensuring the user can focus on relevant sounds such as speech. Traditional software-based digital signal processing (DSP) techniques, while effective, often fall short in meeting the stringent real-time and low-power requirements of hearing aids. This limitation underscores the need for custom VLSI architectures that provide the required speed and efficiency at the hardware level.

The design of VLSI-based filterbanks for hearing aids involves several considerations, including parallelism, low power consumption, and compactness. Parallel processing allows multiple frequency bands to be processed simultaneously, significantly reducing the overall delay. Techniques like pipelining and time-sharing further enhance

the efficiency of these architectures by optimizing the use of hardware resources. Additionally, compact VLSI designs ensure that the hardware fits within the constrained space of a hearing aid, while also minimizing energy consumption to prolong battery life.

One of the most critical aspects of VLSI design for hearing aids is achieving ultra-low power operation. Hearing aids are typically powered by small batteries, which necessitate energy-efficient designs to ensure long-lasting performance. Advanced low-power design techniques, such as clock gating, power gating, and dynamic voltage scaling, are commonly employed in VLSI filterbank architectures to achieve this goal. These techniques reduce power consumption without compromising the processing capabilities of the filterbank, allowing for extended use without frequent battery replacements.

The evolution of VLSI filterbank architectures has also been driven by the need for flexibility and adaptability. Modern hearing aids must cater to a wide range of hearing profiles, which requires the filterbank to be reconfigurable. VLSI technology enables this by allowing the implementation of programmable filterbanks that can be customized based on the user's audiogram. Furthermore, adaptive filterbanks capable of adjusting to dynamic environments, such as noisy streets or quiet rooms, are becoming increasingly popular, further enhancing the user experience.

II. LITERATURE SURVEY

A. K. Samantaray et al.,[1] presents an original calculation and engineering plan for 18-band semi class-2 ANSI S1.11 1/3 octave filterbank. The plan enjoys a few benefits, for example, lower bunch delay, lower computational intricacy, and lower matching mistake. Contrasted and the most recent Liu 's semi class-2 ANSI S1.11 plan, the proposed strategy I (Proposed-I) thoroughly has 72.8% decrease for augmentations per test, 11.25-ms bunch delay, and 59 increments diminished per test.

K. Kaustubh Banninthaya et al.,[2] gives a framework reconfigurable twisted VDF that utilizes a solitary model channel for producing every one of the vital sub-groups. The proposed framework computerizes the age of the control signals for reconfiguring the channel and pipelines the handling of each sub-band to create the essential size reaction.

S. C. Lai, C. H. Liu et al.,[3] presents a clever calculation plan of 18-band semi class-2 ANSI S1.11 1/3 octave channel manage an account with the upsides of low gathering postponement and low intricacy. The proposed strategy uses a straightforward low-pass channel (LPF) and discrete cosine change (DCT) balance to produce a uniform 9-band channel bank first, and afterward move all component of z-1 into all-pass channel to get the non-uniform channel bank to fulfill the guideline.

A. Vijayakumar et al.,[4] shows that the plan measures of p th request investigation having q th request blend channels ($p \neq q$) with an adaptability to control the framework delay has never been tended to correspondingly. In this paper, we propose an efficient plan for a filterbank that can have inconsistent postponement with a (p, q) request. Such filterbanks assume a significant part particularly in applications where low postponement top notch signals are required, similar to a computerized amplifier.

Y. Wei et al.,[5]. the proposed filterbank can accomplish a superior coordinating to the audiogram and has more modest intricacy contrasted and the fixed filterbank. The downside of the proposed strategy is that the throughput delay is somewhat lengthy (>20 ms), which should be additionally decreased before it very well may be utilized in a genuine portable amplifier application.

A. Schasse, et al.,[6] present an effective strategy to build the recurrence goal for discourse improvement calculations in amplifiers. Since the examination amalgamation channel bank applied in computerized listening devices needs to convey a high stop band weakening to empower huge recurrence subordinate intensification gains and a low generally speaking postponement, discourse upgrade frequently experiences the subsequent low recurrence goal.

R. Dong et al.,[7] To assist with creating super low power remote portable hearing assistant items, we examine the incorporation of subband sound coding with amplifier applications. Both the sound coding and the amplifier application use subband handling, yet their prerequisites for the filterbanks are entirely unexpected.

R. Vicen-Bueno et al.,[8] presents the classes, the additional steady increase (ASG) esteem over the breaking point gain of the computerized it is gotten to hear helps. The ASG esteem is accomplished as a tradeoff between the divided sign to-commotion proportion (objective boundary) and the discourse quality (emotional boundary).

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R. Vicen-Bueno, R. Gil-Pita et al.,[9] presents the portrayal of a listening device recreation instrument. This apparatus mimics the genuine way of behaving of advanced DSP-based listening devices fully intent on getting an exceptionally encouraging presentation, which can be utilized for additional plan and examination, and for a superior fitting of the conference weakened patient.

B. Swanson et al.,[10] The Core Opportunity cochlear embed framework empowers a significantly hard of hearing individual to hear. The framework comprises of a precisely embedded trigger and a battery-controlled outer sound processor. The processor depends on a 0.18 µm CMOS ASIC containing four DSP centers.

III. PROPOSED MODEL

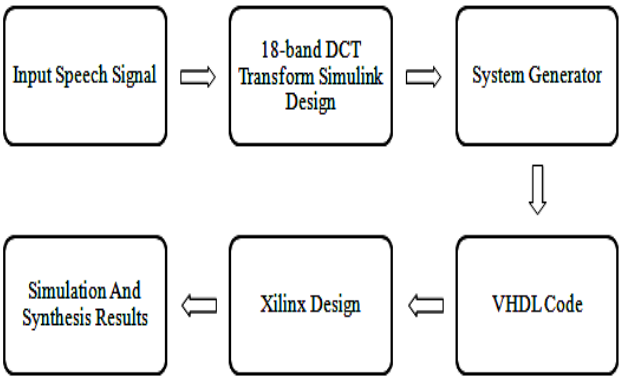

Figure 1: Flow chart

- First to browse the selected input voice signal and then to add the AWGN noise signal. This signal is to allocate the time limitation level.
- Then to select the 1000 limited sample for noisy input selected voice signal. Then to open a simulink model design.
- This simulink design is consists of more no of XILINX based library files and these components are only work to binary based input data bits.
- Our simulink design is consists of gateway in, out and down and up samples, threshold and add component. Then to get the input signal to gateway in component.
- This component is used to convert the analog to digital form. And to apply the low pass and high pass filter decomposition process and to add the threshold function unit.
- Then to apply the low pass filter decomposition section to split the two-level high and low pass filter and to design the 9-step function for decomposition stage.
- Then to design a reconstruction stage, this stage consists of add operator, down sample and high pass filter section. This work is used to reconstruct the original speech data signal.
- Then to select the system generator tool and to convert the simulink design to VHDL code. This code is to represent the hardware structure level.
- Then to simulate the speech denoise architecture and to synthesis the RTL and Technology diagram and to calculate the complexity, time and power level.

IV. SIMULATION RESULTS

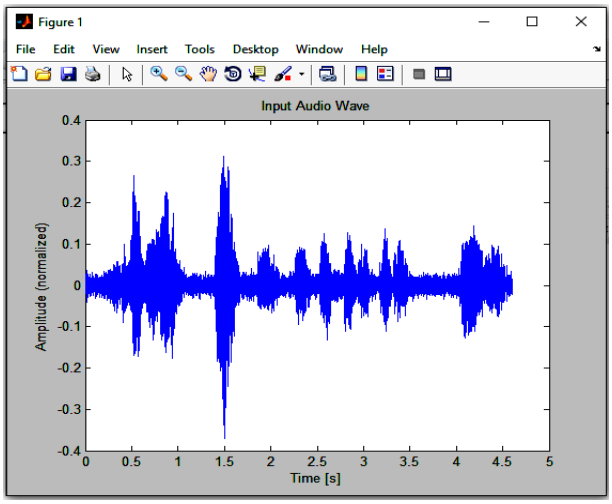

Figure 2: Input audio wave

Figure 2 is presenting the input audio wave; the audio wave is for 5 sec with the maximum amplitude is 04.

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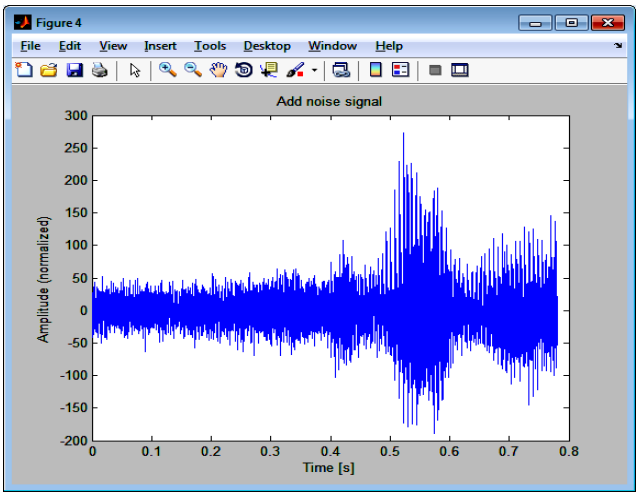

Figure 3: Add noise signal

Figure 3 is presenting the noise added signal waveform where 08. Sec audio wave is taken and add with the noise signal.

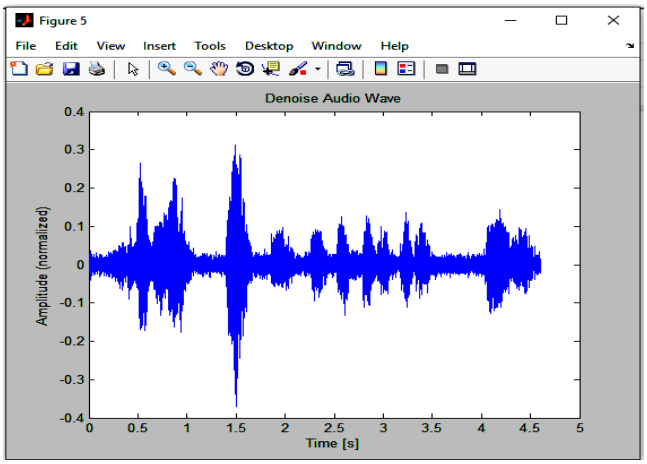

Figure 4: Denoise audio wave

Figure 4 is presenting the denoise signal, the audio wave is proceed through the 18 filterbank in the Simulink and this is control by the VLSI implementation in Xilinx software.

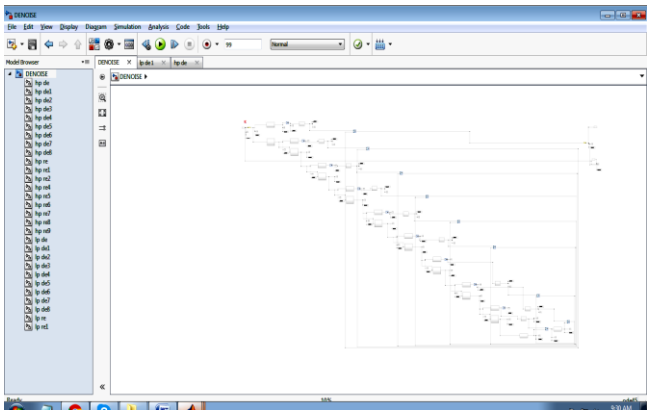

Figure 5: Simulink model

Figure 5 is presenting the Simulink model. Here total 18 filterbank is designed some are the low pass, band pass and high pass filter.

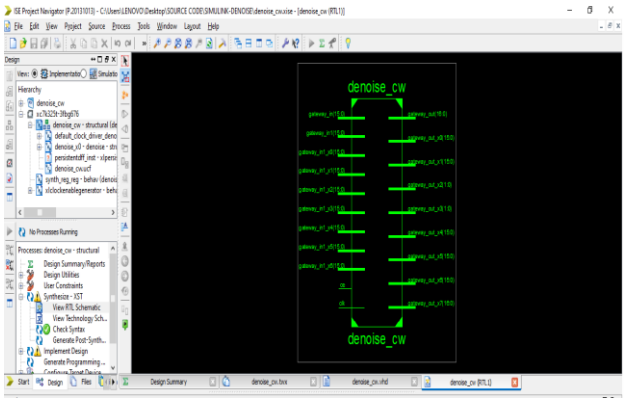

Figure 6: Denoise audio wave

Figure 6 is presenting the denoise continue wave VLSI architecture view. The 18 filter-bank is operated and we check the performance.

Table 1: Result Comparison

Sr No.	Parameter	Previous Work [1]	Proposed Work
1	Delay	11.25-ms	0.678 ns
2	Look Up table	185	160
3	Logic Register	126	67
4	Frequency (MHz)	1380	1474.27

Table 1 is showing comparison of proposed work with previous work. The overall delay is 11.25 ms by the previous and 0.678 ns achieved by the proposed research work. The look up table is 185 in previous and 160 is in proposed. The logic register is 126 in the previous and 67 is in the proposed. The overall frequency is 1380 in previous and 1474.27 is proposed. Therefore the proposed research work is achieving the significant better performance than existing work.

V. CONCLUSION

This research introduces an 18-filter-bank-based VLSI architecture aimed at efficient audio signal processing and noise reduction, specifically addressing the critical demands of low delay and high performance. The proposed architecture is tailored for applications like hearing aids, where real-time audio enhancement is essential for user comfort and functionality. To validate the design, simulations were conducted using MATLAB for algorithm verification and the Xilinx environment for hardware implementation. The Xilinx Virtex-5 FPGA family, known for its high computational power and flexibility, was selected to simulate the hardware performance, ensuring a robust and accurate evaluation. The simulation results reveal that the proposed filter-bank architecture significantly outperforms existing methods in terms of processing speed and latency. The design effectively divides the input audio signal into 18 distinct frequency bands, allowing precise filtering and noise suppression. This ensures enhanced sound clarity while maintaining minimal delay, a critical factor for applications such as hearing aids, where any processing lag can disrupt user experience.

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