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VLSI Architecture of Efficient Wavelet Filter for Image Denoising Computer Vision

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***Abstract*— Wavelet-based filtering is widely recognized as one of the most effective methods for image denoising in computer vision applications. The ability of wavelets to analyze signals at multiple resolutions allows them to effectively separate noise from essential image features, making them ideal for noise reduction tasks. However, the computational complexity of wavelet transforms presents a significant challenge, particularly in real-time applications where speed and power efficiency are paramount. This paper explores the design of efficient Very-Large-Scale Integration (VLSI) architectures for wavelet-based image denoising. It examines the trade-offs between performance, power consumption, and hardware complexity, while analyzing various architectural optimizations such as parallelism, pipelining, and low-power techniques. By reviewing existing VLSI implementations of wavelet filters and identifying their limitations, this study offers insights into how future designs can achieve both high performance and energy efficiency. The paper also discusses the role of field-programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs) in accelerating wavelet-based denoising processes, ultimately providing a roadmap for developing more advanced architectures for computer vision applications.**

Keywords*— *Wavelet, MATLAB, Image, Denoising, VLSI, Filter, Noise, FPGA.

I. INTRODUCTION

Image denoising is a critical preprocessing step in computer vision, used to enhance image quality by removing noise while preserving important details such as edges and textures. Noise can be introduced at various stages of the imaging process, from sensor acquisition to transmission and storage. Reducing this noise without degrading the quality of the image is essential for the successful performance of subsequent tasks such as feature extraction, object recognition, and image segmentation. Among the numerous denoising techniques, wavelet-based filtering has emerged as one of the most effective methods due to its ability to capture both the frequency and location of noise in an image.

Wavelet transforms decompose an image into different frequency components, allowing for multiresolution analysis. This multiresolution capability is highly advantageous in denoising because it enables the selective removal of noise from specific frequency bands while retaining the critical features of the image. The result is a high-quality denoised image that preserves edges and fine details, which are often blurred or distorted by other denoising techniques. Despite its effectiveness, the wavelet transform is computationally intensive, requiring substantial resources for real-time processing. This poses a significant challenge in applications such as autonomous vehicles, medical imaging, and security systems, where low latency and high throughput are essential.

The limitations of software-based implementations for wavelet filtering, particularly in real-time systems, have driven the need for hardware acceleration. Very-Large-Scale Integration (VLSI) architectures offer a solution by enabling the efficient implementation of wavelet-based filters directly in hardware. VLSI designs can take advantage of parallel processing, pipelining, and other optimizations to meet the performance and power efficiency requirements of modern computer vision systems. By offloading the computational workload from general-purpose processors to dedicated hardware, VLSI architectures can achieve real-time performance while maintaining low power consumption.

Designing efficient VLSI architectures for wavelet-based image denoising presents several challenges. First, the computational complexity of the wavelet transform itself must be addressed. Traditional implementations of the discrete wavelet transform (DWT) require a significant number of arithmetic operations, making it difficult to achieve high

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throughput without consuming excessive power or area on a chip. Optimizing the DWT for hardware implementation involves exploring techniques such as parallelism, which allows multiple parts of the image to be processed simultaneously, and pipelining, which enables different stages of the computation to overlap, thereby increasing throughput.

In addition to computational efficiency, the architecture must also be power efficient. Many computer vision applications, such as portable medical devices and drones, are battery-operated and require low-power solutions. Techniques such as clock gating, voltage scaling, and the use of low-power arithmetic units are essential for reducing the power consumption of the VLSI architecture without compromising performance. Additionally, hardware implementations must be scalable to accommodate images of different resolutions and noise levels, as well as flexible enough to support various wavelet functions.

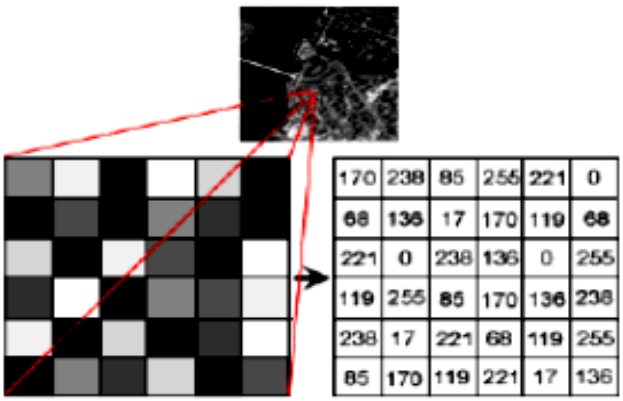

Figure 1: Digital Image

FPGAs and ASICs are two common platforms used for VLSI implementations of wavelet-based image denoising. FPGAs offer reconfigurability, allowing developers to prototype and test different architectures before committing to a final design. Their ability to perform parallel processing makes them well-suited for real-time applications, but they tend to consume more power compared to ASICs. On the other hand, ASICs provide a fixed, highly optimized hardware solution that delivers superior performance and power efficiency but lacks the flexibility of FPGAs. Selecting the appropriate platform depends on the specific requirements of the application, such as the need for rapid development or long-term deployment.

Recent advancements in machine learning and neuromorphic computing are also influencing the design of VLSI architectures for wavelet-based image denoising. Machine learning algorithms, particularly deep learning, have shown promise in improving the accuracy and adaptability of denoising techniques. While deep learning-based denoising is typically implemented in software, integrating these algorithms into VLSI hardware opens up new possibilities for real-time, adaptive noise reduction. Similarly, neuromorphic computing architectures, which mimic the structure and function of the human brain, offer highly parallel and low-power computation that could be leveraged for wavelet-based filtering.

II. PROPOSED METHODOLOGY

The goal of proposed work is to present VLSI based filter for the image denoising.

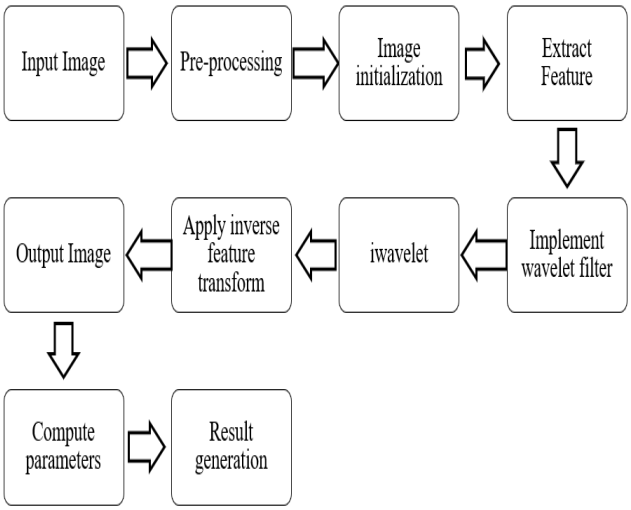

Figure 2: Flow Chart

This flowchart represents the process of applying a wavelet filter for image denoising. Here's a step-by-step description of each block:

1. **Input Image**: The process starts with an input image that requires denoising.

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2. **Pre-processing**: Initial steps applied to the input image to prepare it for further analysis. This may involve noise normalization, contrast adjustments, or other basic corrections.

3. **Image Initialization**: The prepared image is initialized for further processing, such as setting up data structures or transforming the image into a suitable format.

4. **Extract Feature**: This step involves extracting important features from the image, such as edges or textures, which are critical for denoising.

5. **Implement Wavelet Filter**: The wavelet transform is applied to the extracted features. Wavelet filters decompose the image into various frequency components for noise analysis and removal.

6. **iWavelet**: The inverse wavelet transform is applied to reconstruct the denoised image after the noise has been removed or reduced in the feature space.

7. **Apply Inverse Feature Transform**: The image is further processed to reassemble it from the denoised components back into the original spatial domain.

8. **Output Image**: The result of the denoising process is the output image, which ideally has reduced noise while retaining important details.

9. **Compute Parameters**: Any relevant parameters (e.g., signal-to-noise ratio, error metrics) are computed to evaluate the quality of the denoised image.

10. **Result Generation**: Finally, the results, such as the denoised image and performance metrics, are generated for further analysis or output.

III. CHALLENGES

As The simulation is performed using MATLAB and Xilinx software.

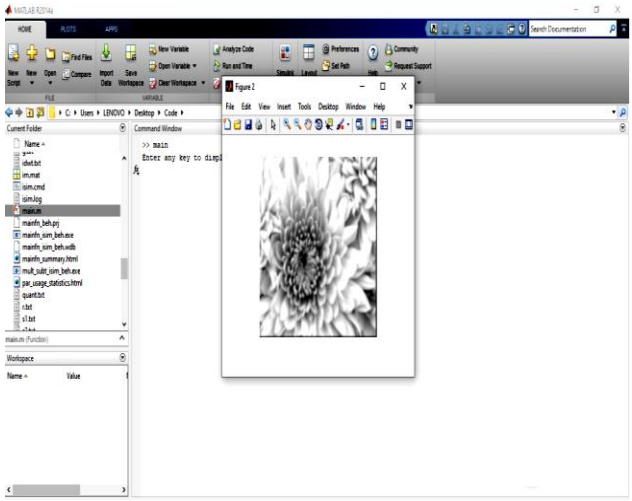

Figure 3: Extract Feature points

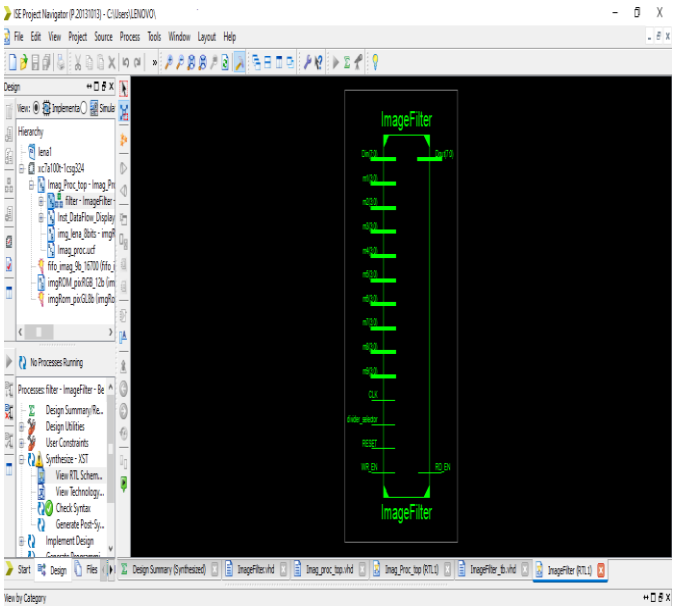

Figure 4: Top module of filter in xilinx environment

Figure 4 is showing the top module of the filter design, where see the various input and output combinations.

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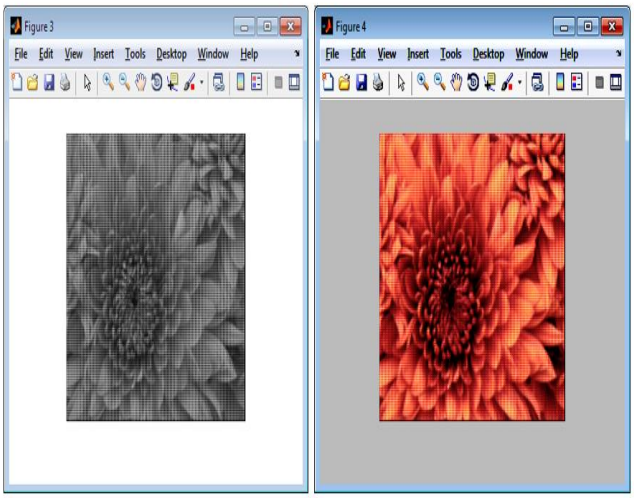

Figure 5: (a) Inverse Transformed Image (B) Output Filtered Image

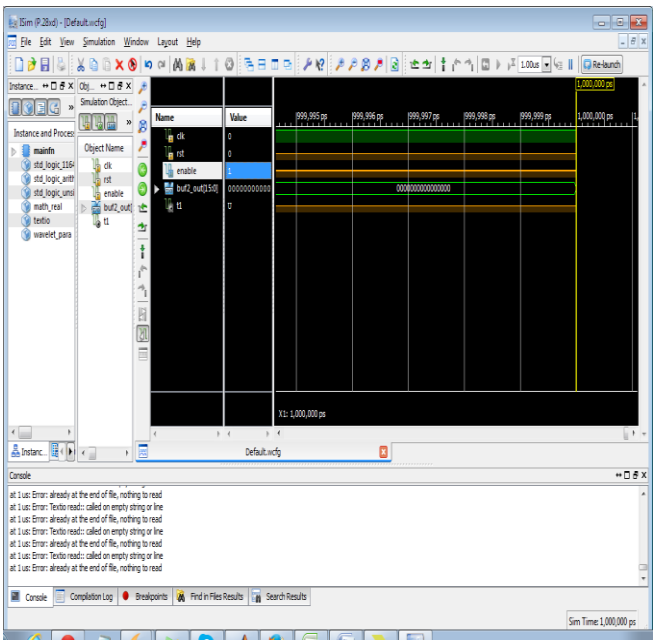

Figure 6: Assign clock and reset

Figure 5 shows the clock and reset pulse, the clock pulse and reset is set at 1 to trigger.

Table 1: Comparison of simulation results

Sr No.	Parameter	Previous Work [1]	Proposed Work
1	Filter Type	Bilateral Filter	Wavelet Filter
2	Delay	NA	0.482 ns
3	Frequency	720 MHz	916.63 MHz
4	Slice look up table	25	13
5	Fully used look up-flip flop pair	12	7
6	Bounded I/O boxes	80	19
7	Throughput	9640 pixels/sec	29332 pixels/sec

Table 1 is showing comparison of proposed work with previous work, so it can be seen that proposed work gives better result than existing work.

IV. CONCLUSION

Image denoising is the technique of removing noise or distortions from an image. The filter architecture is to optimization for improvement in the filtering performance level; reduce the delay level compare to the proposed methodology and to reduce the power consumption also. The filter design is being optimised for an improvement in the level of filtering performance; for a reduction in the level of delay in comparison to the recommended technique; and for a reduction in the level of power consumption as well. The proposed work uses a Wavelet Filter instead of the Bilateral Filter used in prior research, which contributes to significant performance enhancements. Notably, the proposed system achieves a higher operating frequency of 916.63 MHz compared to 720 MHz in the previous work, alongside a low delay of 0.482 ns. The resource utilization is also optimized, with reductions in Slice Look-Up Tables (from 25 to 13), fully used Look-Up Flip-Flop pairs (from 12 to 7), and bounded I/O boxes (from 80 to 19), highlighting a more efficient design. These optimizations result in a substantial increase in throughput, rising from 9640 pixels/sec in the previous work to 29332 pixels/sec in the proposed work, demonstrating its capability for faster processing and better suitability for high-performance applications.

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