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VLSI Architecture of Filterbank with Low Delay for Hearing Aids Application

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***Abstract*— Hearing aids are crucial for individuals with hearing impairments, enabling them to perceive and process sound in a way that mimics natural hearing. A critical component in hearing aids is the filterbank, which decomposes incoming audio signals into various frequency bands, allowing for precise amplification and filtering. However, hearing aids must operate with minimal delay to ensure that sound processing occurs in real-time, aligning with the user's expectations for natural sound perception. Achieving low delay in the filterbank while maintaining high signal fidelity poses a significant challenge, particularly in the resource-constrained environment of hearing aid devices. This paper explores the design and optimization of VLSI (Very Large-Scale Integration) architectures for low-delay filterbanks tailored for hearing aid applications. The review focuses on techniques to reduce computational complexity, minimize power consumption, and achieve real-time performance, ensuring that the hearing aids provide optimal audio quality and user experience.**

Keywords*— *Filterbank, Wavelet, VLSI, Channel, Delay, Complex, Hearing Aid.

I. INTRODUCTION

Hearing aids have become indispensable devices for millions of individuals with hearing impairments, helping them regain the ability to perceive and interact with the auditory world. One of the most important components of a hearing aid is the filterbank, a system that decomposes incoming sounds into various frequency bands. This process allows the hearing aid to amplify specific frequencies that are most affected by the user's hearing loss while maintaining the overall sound quality. However, the implementation of an efficient filterbank in hearing aids is not without challenges, particularly when it comes to achieving low latency—a critical feature for real-time auditory perception.

Achieving low delay in signal processing is crucial for hearing aids because the human brain is highly sensitive to timing discrepancies in sound. A noticeable delay between the actual sound and the processed output can create a sense of dissonance, resulting in discomfort for the user. This becomes particularly problematic when individuals are engaged in real-time conversations or interacting with sound-visual stimuli, such as watching TV or communicating face-to-face. Therefore, minimizing delay is essential for creating a natural and seamless auditory experience for hearing aid users.

The filterbank structure in a hearing aid divides the input sound signal into multiple frequency bands to process and amplify them selectively. This is especially important because hearing loss does not typically affect all frequencies equally—many people have more difficulty hearing higher frequencies than lower ones. Filterbanks allow hearing aids to target these frequency-specific hearing losses effectively. However, implementing these filterbanks in hardware requires careful consideration to minimize delay while still achieving accurate and high-quality sound processing.

Designing VLSI architectures for hearing aids presents unique challenges due to the competing demands of low power consumption, small form factors, and real-time performance. VLSI enables the integration of complex signal processing functions, such as filterbanks, onto a single chip, but this comes with constraints on how fast and efficiently these operations can be executed. For hearing aids, the VLSI architecture must be designed to process audio signals with minimal delay while conserving power, as hearing aids are typically battery-operated.

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Several techniques have been explored to optimize VLSI architectures for low-delay filterbanks in hearing aids. Parallel processing and pipelining are commonly employed strategies that allow different parts of the signal processing to occur simultaneously or in overlapping stages, reducing the overall processing time. Additionally, methods such as clock gating and dynamic voltage scaling help minimize power consumption, ensuring that the hearing aid can operate efficiently for extended periods without frequent battery replacements.

While these design optimizations improve performance, there are inherent trade-offs between delay, complexity, and power efficiency. For instance, more complex filterbanks can provide better frequency resolution and signal fidelity, but they also tend to introduce longer delays and higher computational demands. Balancing these trade-offs is key to developing a filterbank that offers both low delay and high sound quality, while still meeting the strict power and size constraints required for hearing aids.

II. METHODOLOGY

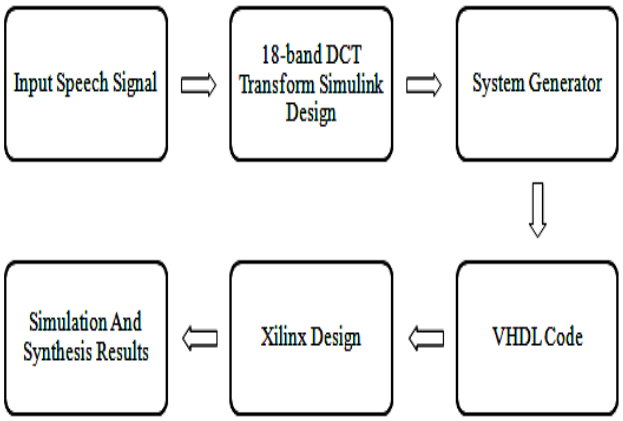

Figure 1: Flow chart

The flow chart you provided illustrates a process for designing and simulating a Discrete Cosine Transform (DCT) filterbank for speech signal processing, specifically with an 18-band structure. Here's a detailed description of each stage:

1. **Input Speech Signal**: This is the raw audio signal that serves as the input for the system. It typically contains spoken words or sound data that needs to be processed.

2. **18-band DCT Transform Simulink Design**: The input speech signal is processed using an 18-band Discrete Cosine Transform (DCT) filterbank. This step occurs within Simulink, a model-based design environment used for dynamic system simulation. The 18-band DCT splits the input signal into 18 frequency bands, allowing for efficient frequency-domain processing of the speech signal.

3. **System Generator**: After designing the DCT in Simulink, the System Generator is used. This is a tool often used for translating Simulink models into hardware descriptions, suitable for digital implementation. It generates the hardware design that will eventually be synthesized into hardware logic.

4. **VHDL Code**: Once the system generator completes its process, it outputs the design in VHDL (VHSIC Hardware Description Language). VHDL is a hardware description language used to model and describe digital systems at various levels of abstraction. This VHDL code is ready for synthesis and hardware implementation on FPGAs (Field-Programmable Gate Arrays) or other hardware platforms.

5. **Xilinx Design**: The generated VHDL code is taken into the Xilinx design suite (e.g., Xilinx ISE or Vivado), where it is further processed for FPGA synthesis. This step involves compiling, optimizing, and mapping the design to the specific FPGA architecture, preparing it for simulation or real-world deployment.

6. **Simulation and Synthesis Results**: Once the design has been mapped to the hardware using the Xilinx tools, the simulation results are obtained to evaluate how the system performs. These results provide insights into the filterbank's performance, accuracy, delay, and efficiency. The synthesis results are used to determine if the design meets the target hardware's requirements for area, power, and timing.

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III. SIMULATION AND RESULTS

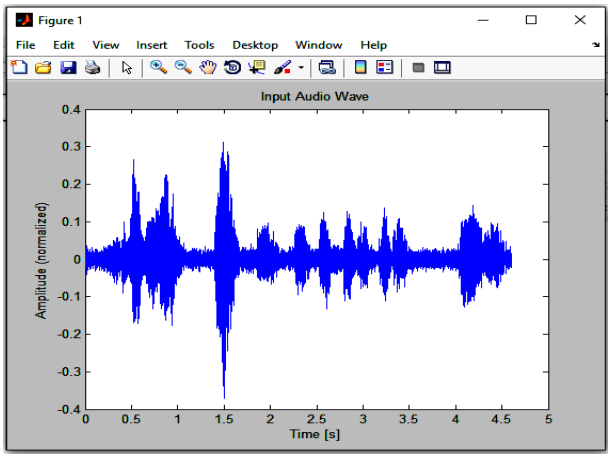

Figure 2: Input audio wave

Figure 2 is presenting the input audio wave; the audio wave is for 5 sec with the maximum amplitude is 04.

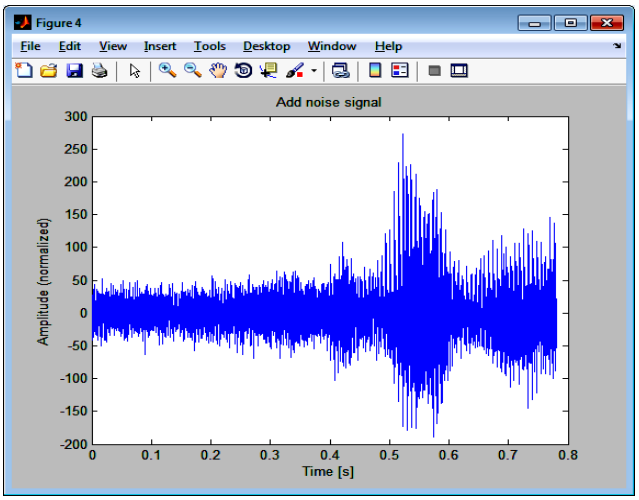

Figure 3: Add noise signal

Figure 3 is presenting the noise added signal waveform where 08. Sec audio wave is taken and add with the noise signal.

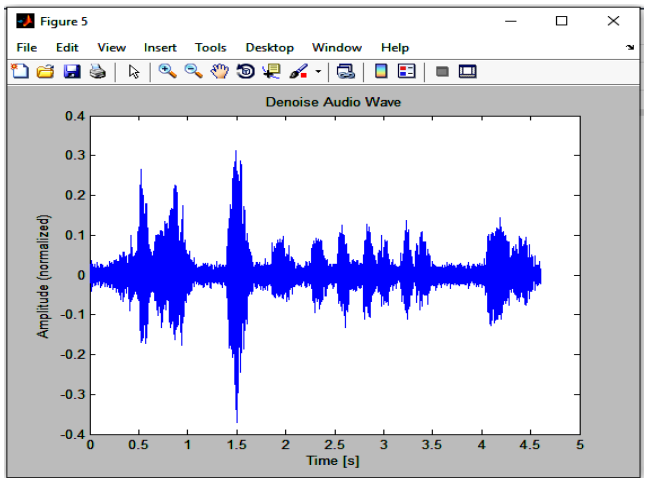

Figure 4: Denoise audio wave

Figure 4 is presenting the denoise signal, the audio wave is proceed through the 18 filterbank in the Simulink and this is control by the VLSI implementation in Xilinx software.

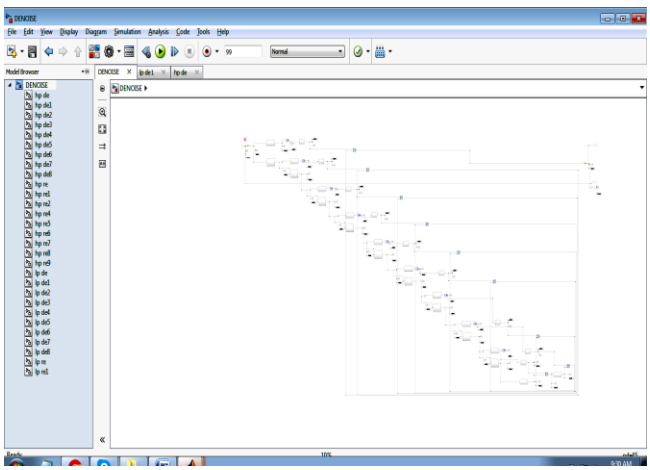

Figure 5: Simulink model

Figure 5 is presenting the Simulink model. Here total 18 filterbank is designed some are the low pass, band pass and high pass filter.

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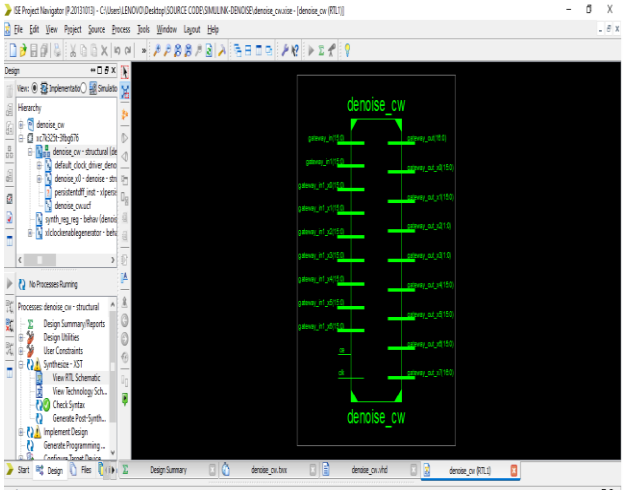

Figure 6: Denoise audio wave

Figure 6 is presenting the denoise continue wave VLSI architecture view. The 18 filter-bank is operated and we check the performance.

Table 1: Comparison of simulation results

Sr No.	Parameter	Previous Work [1]	Proposed Work
3	Delay	11.25-ms	0.678 ns
4	Look Up table	185	160
5	Logic Register	126	67
6	Frequency (MHz)	1380	1474.27

Table 1 is showing comparison of proposed work with previous work. The overall delay is 11.25 ms by the previous and 0.678 ns achieved by the proposed research work. The look up table is 185 in previous and 160 is in proposed. The logic register is 126 in the previous and 67 is in the proposed. The overall frequency is 1380 in previous and 1474.27 is proposed. Therefore the proposed research work is achieving the significant better performance than existing work.

IV. CONCLUSION

This research proposed the 18 filter-bank based VLSI architecture for the audio signal processing or denoisng. The simulation is successfully done using MATLAB and the Xilinx environment. Vertex 5 families are used to simulate the research work. The simulation results show that the proposed research work is achieving the significant better performance than existing work.

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