International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347 - 6435 (Online) Volume 13, Issue 10, October 2024)

Secure and Efficient Lightweight AES Algorithms for IoT Applications

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***Abstract*— With the rapid growth of the Internet of Things (IoT), ensuring data security in resource-constrained devices has become a critical challenge. The Advanced Encryption Standard (AES), a widely adopted cryptographic algorithm, provides robust data security but often demands significant computational resources. This presents a challenge for IoT devices with limited power, memory, and processing capabilities. In response, lightweight versions of AES have been developed to meet the specific needs of IoT environments. These lightweight AES algorithms maintain the strong security properties of standard AES while optimizing efficiency in terms of speed, energy consumption, and resource usage. This paper presents a comprehensive review of lightweight AES algorithms tailored for IoT applications, focusing on their design principles, performance, and trade-offs. We also analyze their applicability in various IoT use cases, emphasizing the importance of balancing security and efficiency in IoT deployments.**

Keywords*— *Secure, Lightweight, AES Algorithms, IoT.

I. INTRODUCTION

The Internet of Things (IoT) has emerged as a transformative technological paradigm, interconnecting billions of devices worldwide. From smart homes and wearable devices to industrial automation and healthcare systems, IoT has the potential to revolutionize daily life and industries. However, the ubiquity of connected devices also introduces significant security risks, as IoT networks often handle sensitive data and operate in critical environments. Ensuring the security and privacy of data in such systems is paramount, particularly when these devices are highly constrained in terms of computational power, energy resources, and memory capacity.

Among the most commonly used cryptographic standards is the Advanced Encryption Standard (AES), which was selected by the National Institute of Standards and Technology (NIST) in 2001 as a robust, highly secure encryption method. AES offers strong resistance against most known cryptographic attacks, making it the gold standard for securing communications in a wide range of applications, from financial services to government data protection. However, the design of AES, while highly secure, was optimized for systems with ample resources. As IoT devices are often constrained by hardware limitations such as low processing power, limited battery life, and small memory footprints, standard AES can be too resource-intensive for direct application in many IoT scenarios.

This challenge has given rise to the development of lightweight cryptographic algorithms, specifically lightweight variants of AES, which are designed to provide a balance between security and efficiency. These lightweight AES algorithms aim to maintain the high security standards of AES while reducing the algorithm's complexity and resource consumption to make it suitable for IoT devices. The need for such algorithms is especially acute in applications where devices operate autonomously for extended periods without direct human intervention, such as in remote sensing or environmental monitoring systems, where frequent battery replacement is not feasible.

The primary goal of lightweight AES algorithms is to reduce the number of operations, memory requirements, and power consumption, without compromising the cryptographic strength of the encryption. By doing so, these algorithms enable secure communication across IoT networks without overwhelming the limited capabilities of the devices involved. For instance, lightweight AES variants might simplify the number of rounds in the encryption process, optimize key schedules, or utilize hardware accelerators that are better

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suited for constrained environments. Despite these optimizations, designing lightweight AES algorithms is not without its challenges, as reducing resource usage often introduces trade-offs in areas such as encryption speed or potential vulnerability to side-channel attacks.

As the IoT landscape continues to evolve, the demand for secure and efficient cryptographic solutions will only increase. This is particularly true as IoT applications extend into critical infrastructure sectors such as healthcare, transportation, and energy, where data security is not only a matter of privacy but also of safety. In such environments, lightweight AES algorithms can play a crucial role by enabling secure, real-time communication while conserving the limited resources available to IoT devices. The importance of these algorithms extends beyond merely reducing resource consumption; they are vital to ensuring that even the most resource-constrained devices can maintain high standards of data security in increasingly complex IoT networks.

II. PROPOSED METHODOLOGY

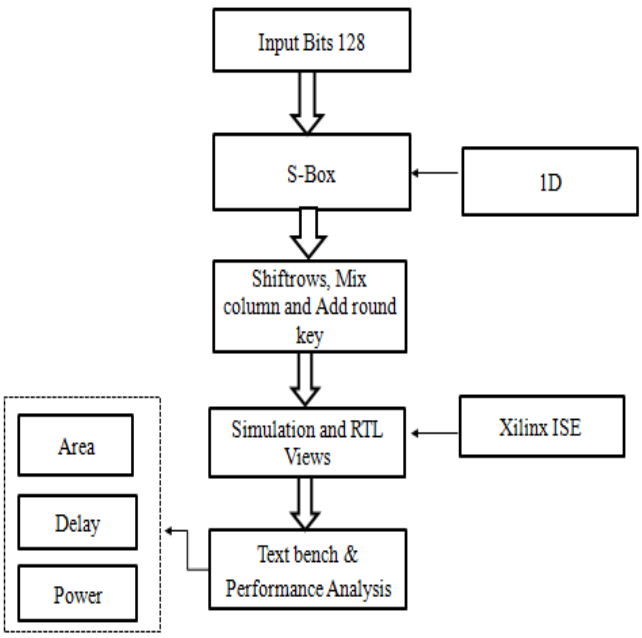

Figure 1: Flow chart

The flowchart you've provided outlines the process for implementing and analyzing a cryptographic algorithm, most likely AES (Advanced Encryption Standard), on a hardware platform using tools like Xilinx ISE (a tool for FPGA development). Here's a detailed description of the process step-by-step:

1. Input Bits 128

- **Description**: The algorithm begins by taking a 128-bit input, which is the block size for AES encryption. AES operates on 128-bit blocks, and this step involves receiving or formatting the input data into 128 bits for processing.

2. S-Box

- **Description**: The **S-Box (Substitution Box)** is a non-linear substitution step in AES. It is used for substituting bytes in the input data according to a predefined table, improving security by introducing confusion into the data. In this flow, the 128-bit input is passed through the S-Box transformation.
- **1D**: Likely refers to a one-dimensional lookup table used to implement the S-Box, which performs byte substitution on each byte of the input data.

3. Shiftrows, Mixcolumn, and Add Round Key

- **Description**:
  - **ShiftRows**: This is a step in AES where the rows of the state (the input after S-Box) are cyclically shifted by different offsets. It adds diffusion to the algorithm.
  - **MixColumns**: In this step, columns of the state are mixed using a mathematical transformation, enhancing diffusion.

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- **AddRoundKey**: This step XORs the state with a round key derived from the original encryption key. This step ties the encryption process to the secret key, ensuring security.

4. Simulation and RTL Views

- **Description**:
  - **Simulation**: At this stage, the AES algorithm (which includes the S-Box, ShiftRows, MixColumns, and AddRoundKey) is simulated to verify that the encryption process is working correctly.
  - **RTL Views**: RTL (Register Transfer Level) design is a hardware description of the AES algorithm. It represents the hardware implementation of the cryptographic process. Viewing RTL allows for insight into how the logic is designed in terms of flip-flops, logic gates, and connections.

5. Xilinx ISE

- **Description**: This refers to the use of **Xilinx ISE** software, which is used for synthesizing and implementing the AES algorithm on FPGAs (Field Programmable Gate Arrays). It converts the RTL description into a hardware implementation on a specific FPGA device.

6. Text Bench & Performance Analysis

- **Area**: The amount of FPGA resources (e.g., logic gates, flip-flops) used to implement the AES algorithm.
- **Delay**: The time taken for the algorithm to process the input data and generate the output (latency).
- **Power**: The amount of power consumed by the hardware implementation of AES, which is crucial for IoT applications where power consumption is often limited.

7. Overall Flow:

- The flow begins with a 128-bit input that goes through the S-Box for substitution.
- Then, the data is transformed further using ShiftRows, MixColumns, and AddRoundKey.
- The entire process is simulated and synthesized into hardware using RTL design in Xilinx ISE.
- Finally, the performance of the AES implementation is analyzed by measuring area, delay, and power using a test bench.

III. SIMULATION AND RESULTS

Nano AES Security Algorithm implementation has multiple sub-modules inside it both at the Encryption and Decryption end, based on the internal operations of the algorithm.

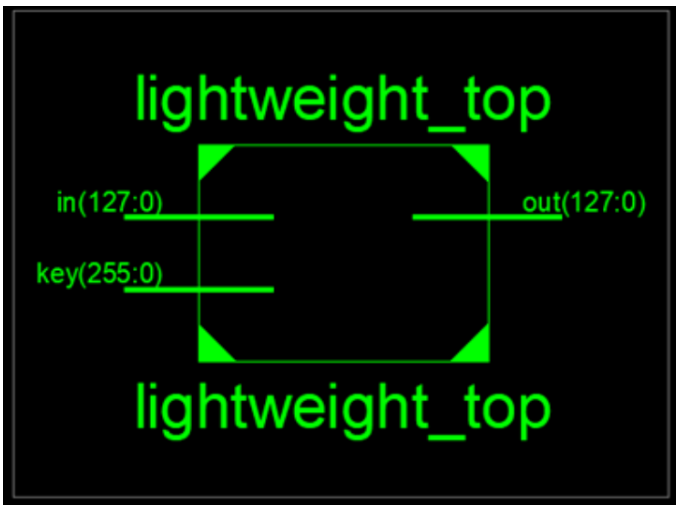

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Figure 2: Top View

In figure 2, top view of proposed Nano-AES lightweight cryptography algorithm, where 128-bit input, 128-bit output and 256 Encryption and 256 Decryption key taken.

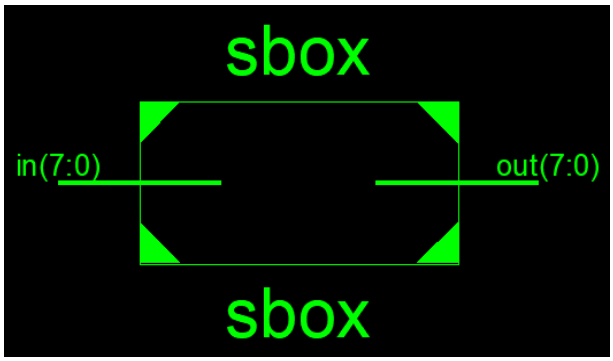

Figure 3: Top module of proposed 1D S-box

Figure 3 is showing the top module of the proposed 1-dimensional sub-byte box. Here 8-bit input is giving to the Sbox and its generating 8-bit output after operation of s-box.

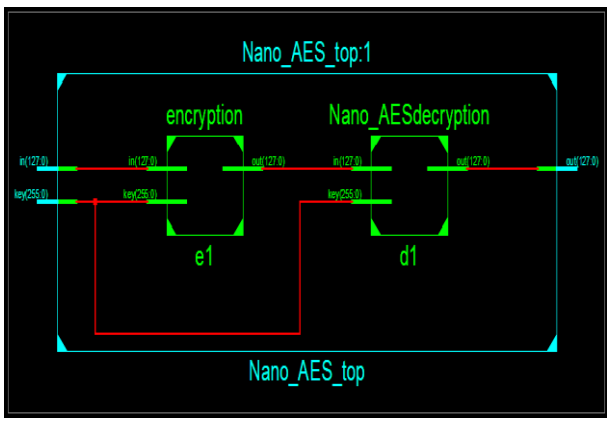

Figure 4: RTL view of Encryption and Decryption Process

The figure 4 is showing the RTL view of encryption and decryption process. The 128-bit input data is encrypted by the 256-bit key and at the output side it is decrypted by same 256 bit key and original data is recovered.

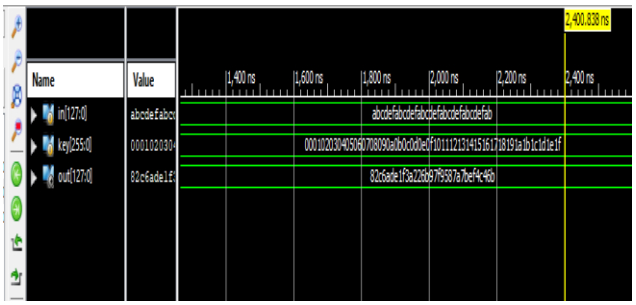

Figure 5: Encryption process

Figure 5 presents the encryption process of the proposed Nano-AES lightweight cryptography algorithm.

Input – abcdefabcdefabcdefabcdefabcdefab

Key-
h000102030405060708090a0b0c0d0e0f1011121314
15161718191a1b1c1d1e1f

Output - 82c6ade1f3a226b97f9587a7bef4c46b

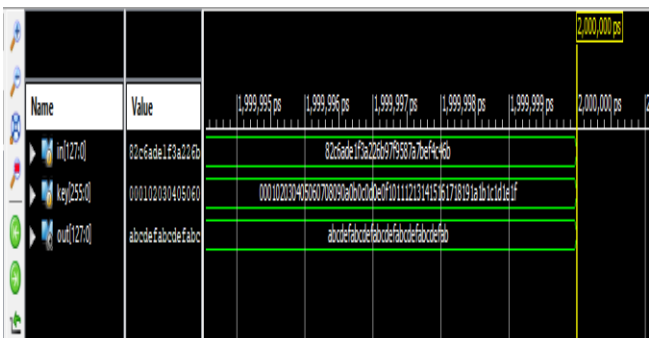

Figure 6: Decryption Process

Figure 6 presents the decryption process of the proposed Nano-AES lightweight cryptography algorithm.

Input – 82c6ade1f3a226b97f9587a7bef4c46b

Key-
h000102030405060708090a0b0c0d0e0f1011121314
15161718191a1b1c1d1e1f

Output – abcdefabcdefabcdefabcdefabcdefab

Table 1: Result Comparison

Sr No	Parameters	Previous Result	Proposed Result
1	Method	AES	Nano AES
2	Input bit	128	128
3	S Box	4 x 4	1X8
4	Chip area	13340	13016
5	Frequency	238.10 MHz	284.10 MHz
6	Delay	41.99ns	3.52ns

IV. CONCLUSION

This paper presents novel high performance of nano AES for lightweight implementation in IoT & AI Devices. Both methods utilize a 128-bit input size, but the Nano AES achieves greater efficiency with a more compact 1x8 S-Box configuration compared to the 4x4 S-Box in standard AES. This optimization leads to a reduced chip area, with the Nano AES occupying 13016 units versus 13340 units for the traditional AES, making it more suitable for space-constrained environments. The Nano AES also operates at a significantly higher frequency of 284.1 MHz compared to 238.10 MHz, allowing for faster data processing. Most notably, the delay is reduced from 41.99 ns in the traditional AES to just 3.52 ns in the Nano AES, indicating a substantial improvement in processing speed. These results underscore the Nano AES's suitability for high-performance, resource-efficient applications in IoT and AI devices.

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