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Design of Ultra-Low Power Multiple Transistor with Single-Phase Clocked Flip-Flop for IoT Applications

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***Abstract*— In the era of the Internet of Things (IoT), energy-efficient and ultra-low-power circuits are crucial to extending the battery life of devices and enabling sustainable, long-term deployments. This paper presents the design of an ultra-low-power multiple transistors with a single-phase clocked flip-flop, tailored specifically for IoT applications. The proposed flip-flop utilizes a minimal transistor count while maintaining optimal performance, ensuring low power consumption and reduced area overhead. The innovative design approach addresses the challenges of conventional flip-flops, such as power leakage and clocking complexity, by employing a single-phase clocking scheme, which simplifies the clock network and reduces dynamic power consumption. The proposed flip-flop design is simulated using industry-standard CMOS technology, and the results demonstrate its superiority in terms of power efficiency, delay, and area compared to traditional designs.**

***Keywords*— TSPC, Clock, FPGA, IOT, Transistor .**

I. INTRODUCTION

The rapid advancement of IoT technology has transformed the way we interact with the world, connecting a wide range of devices and enabling seamless data exchange in real-time. From smart homes to industrial automation, IoT devices are increasingly becoming an integral part of modern life. However, one of the key challenges in IoT design is managing power consumption. Since many IoT devices operate in remote or hard-to-reach locations, they rely heavily on battery power or energy harvesting techniques, making energy efficiency a critical concern.

In the context of IoT applications, flip-flops play a vital role as fundamental building blocks in digital circuits. They are used in memory elements, data storage, and sequential logic circuits. Traditional flip-flop designs, while effective in many high-performance applications, are not ideal for IoT systems, where power consumption is a primary constraint. The need for continuous operation and the limitation of energy resources in IoT devices necessitate the development of flip-flops that consume ultra-low power, have minimal area overhead, and can function efficiently with reduced clocking complexity.

Conventional flip-flop designs typically employ multi-phase clocking schemes, which require complex clock distribution networks and lead to higher dynamic power consumption. These designs also often include a large number of transistors, contributing to both increased power consumption and larger chip areas. The complexity of the clocking scheme further results in clock skew and increased power dissipation, making these designs suboptimal for energy-constrained environments like IoT devices.

To address these challenges, this paper proposes an ultra-low-power multiple transistor flip-flop design with a single-phase clocking scheme, specifically tailored for IoT applications. The use of a single-phase clock significantly reduces the power consumed in the clock distribution network, while the minimalist transistor design ensures low leakage power and reduced area. This innovative approach not only simplifies the clocking structure but also decreases dynamic power consumption, making the flip-flop highly suitable for ultra-low-power IoT applications.

The proposed design is implemented using Complementary Metal-Oxide-Semiconductor (CMOS)

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technology, which is widely used in low-power digital circuits. CMOS technology is particularly advantageous for IoT applications due to its inherent low power dissipation in static conditions. By leveraging CMOS technology, the proposed flip-flop achieves minimal power leakage and improved energy efficiency.

II. METHODOLOGY

The methodology of proposed work is as follows-

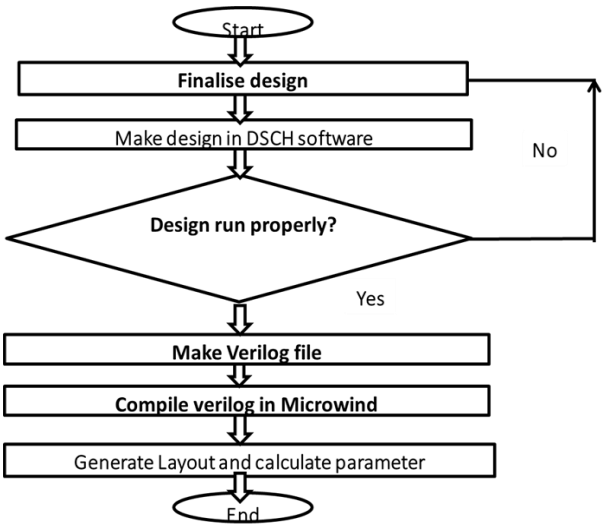
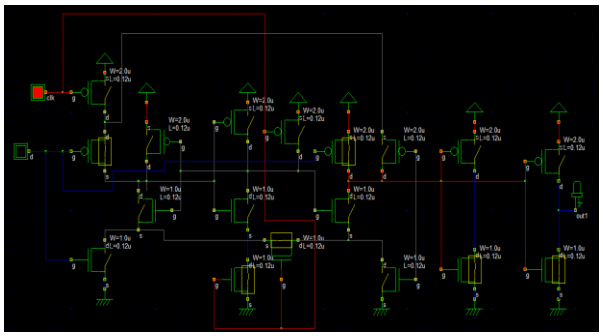


Figure 1: Flow chart

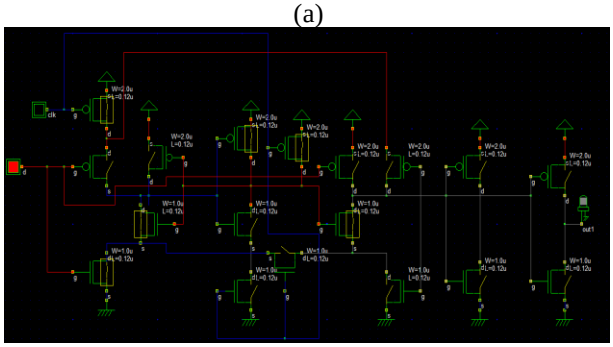
This work proposes 18-semiconductor SPC (18TSPC), a SPC FF with just 18 semiconductors (the least detailed for a completely static conflict free SPC FF) with a clever expert slave Fig. 3. Reproduction results show TCFF inner hub voltages at (a) VDD = 1.2 V and (b) VDD = 0.6 V while D ascending at CK = 0 [15]. geography With an improved on geography, it conveys a 20% decrease in cell region contrasted with TGFF. Not at all like SoA plans, 18TSPC meets generally super low power FF plan prerequisites. It has been carried out in 65-nm CMOS alongside a TGFF. This demonstrates EDA similarity and shows circuit and framework level advantages. The plan was first recreated then tentatively approved at 0.7 V, 25 ◦C, at different information action rate (α), showing that the proposed 18TSPC accomplishes decreases of 68% and 73% in generally (Pα=10%) and clock dynamic power (Pα=0%), individually, and 27% lower spillage contrasted with TGFF. Moreover, not at all like TCFF, the estimations demonstrate prevalent 18TSPC in execution.

SPC FF Configuration Approach The point of the plan is to convey forward the upgrades accomplished by recently detailed FFs regarding cell region, power utilization, and execution yet to beat the impediments of these plans. To do this, the underlying advance is to assess the Boolean capacity of a positive-edge trigged ace slave FF (MSFF) Dpresent ML = CK • D + CK • Dprevious ML (1) Dpresent SL = CK • Dprevious SL + CK • Dpresent ML (2) In (1), D is the information input, Dpresent ML is the current information in the expert lock, and Dprevious ML is the information which has been hooked from D during the past low CK. In (2), Dpresent SL is the current information in the slave lock and Dprevious SL is the information which has been hooked from the result of the expert hook during the past high CK in the slave hook.

III. SIMULATION RESULTS



(a)



(b)

Figure 2: Proposed 18-TSPCFF and output-2

Figure 2 introducing, 18-TSPCFF when clk=1 d=0 and out=0, and when clk=0, d=1 then output=1.

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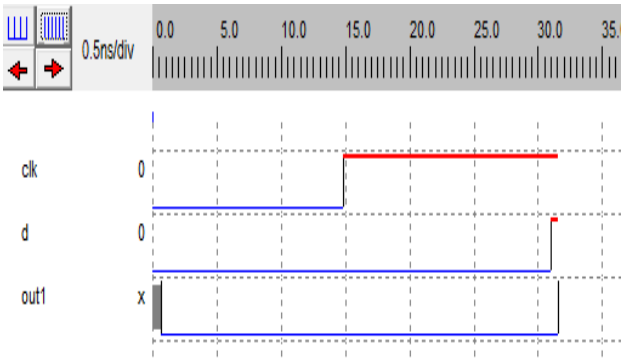

Figure 3: Timing diagram of 18-TSPCFF

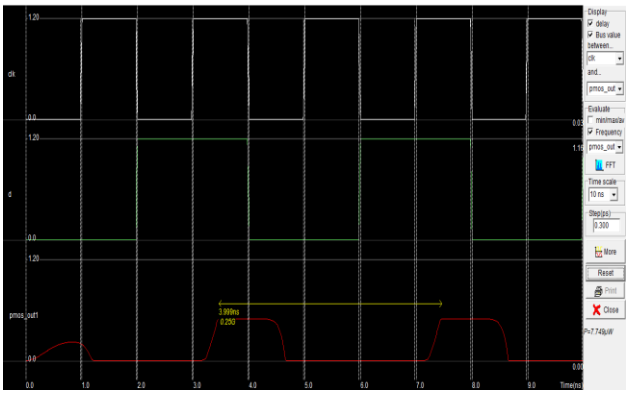

Figure 4: Voltage vs time of 18-TSPCFF

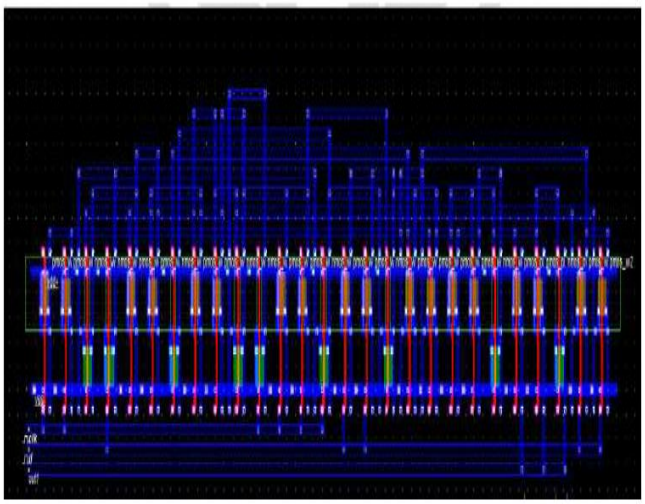

Figure 5: Layout of 18-TSPCFF

Table 1: Result Comparison

S.N	Parameter	Previous	Proposed
		Work	Work
1	Design	19-TSPC	18-TSPC
2	Topology	Gate level	Compressed Topology
3	Area (um^2)	3265	374
4	Power(uW)	30	6.54
5	Delay (ns)	13.28	7
6	Rise Time(ns)	9.2	0.25
7	Fall Time(ns)	11	0.25

IV. CONCLUSION

This paper proposed 18TSPC, a fully static and contention free SPC FF with the lowest reported number of transistors (18), demonstrating a significant cell area reduction with respect to the conventional TGFF. Although a performance penalty is observed, thanks to the low-power characteristic of the proposed design, 18TSPC achieves more. A brief summary of the proposed 18TSPC and comparison with prior works is presented. Therefore the proposed 18TSPC has better power characteristics than the previous. Design of this research work is 18-TSPC using 50 nm technologies. Proposed designs used compressed topology. The utilization area is 374 mm2. The power consumption of designs is 6.54 uW. The delay of 7 nS. The setup and hold time are 0.25nS.

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