Reversible Logic based Adder-Sub for High Speed Arithmetic Applications: A Review

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Abstract— **Reversible logic is a critical area of research with significant potential for enhancing energy efficiency and performance in digital systems, particularly in high-speed arithmetic applications. Traditional logic circuits dissipate power due to information loss, making them inefficient for future computing technologies like quantum computing, cryptography, and low-power VLSI design. Reversible logic, on the other hand, ensures that no information is lost, leading to a reduction in heat dissipation and power consumption. This review explores the use of reversible logic in the design of adder-subtractor units for high-speed arithmetic operations.**

Keywords— *Reversible, Adder, Subtractor, Arithmetic.*

I. INTRODUCTION

In today's world of high-performance computing, energy efficiency has become a top priority. As computing power increases, so does the demand for efficient arithmetic circuits capable of performing high-speed operations while consuming minimal power. Traditional logic circuits, which are based on irreversible logic, generate significant heat due to energy dissipation. This energy loss becomes particularly concerning as the scale of circuits increases in applications like VLSI design, cryptography, and quantum computing.

To address these challenges, reversible logic has emerged as a powerful alternative to traditional irreversible logic. A reversible logic circuit is one in which the input can be uniquely reconstructed from the output, ensuring that no information is lost during computation. This means that reversible circuits, in theory, dissipate zero energy and are thus ideally suited for energy-efficient designs. In addition, reversible logic plays a key role in quantum computing, where

computation is naturally reversible, and quantum gates inherently obey reversible logic principles.

Arithmetic operations such as addition and subtraction form the backbone of most computational tasks. As applications like real-time data processing, signal processing, and cryptographic algorithms require ever-increasing processing speeds, the design of efficient arithmetic circuits has become crucial. In this context, adders and subtractor units are integral components of processors and digital signal processors (DSPs). The performance of a computational system is often determined by how efficiently these basic arithmetic operations are executed.

Traditional adders and subtractors, while highly optimized, suffer from certain limitations when it come to power dissipation and speed. The need to propagate carry bits across several stages in adders leads to delays, while information loss in both adders and subtractors results in unnecessary energy consumption. This has driven researchers to explore alternative design methodologies, such as carry-lookahead adders (CLAs) and parallel prefix adders, which can reduce the critical path delay. However, these designs are still based on irreversible logic and thus face limitations in terms of power efficiency.

Reversible logic-based arithmetic circuits offer a novel approach to address these challenges. By ensuring that no information is lost during computation, reversible circuits are inherently more power-efficient than their irreversible counterparts. Additionally, reversible logic enables the design of circuits that can perform both addition and subtraction operations using the same hardware, further enhancing the flexibility and efficiency of arithmetic units.
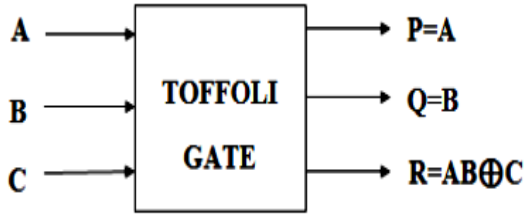
Figure 1: Toffoli Gate

The concept of a reversible adder-subtractor involves designing a circuit where the operation mode (addition or subtraction) can be toggled based on a control signal, all while ensuring that the input information can be fully recovered from the output. This reduces the need for separate hardware implementations for adders and subtractors, which in turn decreases the overall circuit complexity and power consumption.

Various reversible gates, such as the Toffoli gate, Fredkin gate, Peres gate, and Feynman gate, have been used to design reversible arithmetic circuits. These gates differ from traditional logic gates in that they maintain a one-to-one mapping between inputs and outputs, ensuring reversibility. For instance, the Toffoli gate, which is a universal reversible gate, can be used to implement Boolean functions like XOR, which is critical for designing adders.

II. LITERATURE SURVEY

N. S, et al., [1] presented a new exact reversible full adder has a 'quantum cost' (QC) of 9 with total delay of 7Δ. The proposed adder herein referred to as "Exact Reversible Full Adder" (ERFA). The proposed ERFA is designed using 4-Feynman gates and 1-Fredkin gate in three different stages. The proposed ERFA has '2' ancillary inputs (AIs) and '3' garbage outputs (GOs). Further, to verify the functionality, the proposed ERFA is designed and validated through Verilog HDL code simulation. Also, it is compared in terms of various design metrics (DMs) against 16 reversible full adders that were reported in the current literature.

A. Anjana et al., [2] The reversible logic gates are the most eminent enabled technology for energy efficient system realization. This paper introduced a unified reversible logic gate called HAS [2] gate for performing arithmetic addition/subtraction and swap operations. The designed gate can also perform other Boolean functions as copy, NOT, AND, Exclusive-OR and Exclusive-NOR. The proposed gate is compared with other existing gates regarding quantum cost, garbage values and count of reversible gates.

S. Majumder et al., [3] presented, circuits with low power and less computation time are in high demand in VLSI technology. In this context, the applications of reversible logic are far-reaching. In this paper, the detailed evaluation of certain reversible gates, namely, Feynman gate, Peres Gate, Modified Fredkin Gate, Modified Toffoli Gate, and TS Gate is set forth. Evaluation comprises of transistor implementation, simulation results and average power and delay measurement.

M. Awais, et al., [4] Reversible logic is an emerging digital design paradigm which promises low energy dissipation; thanks to its information-lossless nature. True potential of this exciting concept can only be assessed by facing the design of practical complexity applications. Low density parity check (LDPC) decoding is one such application from forward error correction domain. The core of LDPC decoding is the check node (CN) processor, which executes the decoding algorithm and constitutes a major portion of decoder's overall power consumption.

C. Bandyopadhyay et al., [5] reversible logic synthesis is one of the best suited ways which act as the intermediate step for synthesising Boolean functions on quantum technologies. For a given Boolean function, there are multiple possible intermediate representations (IRs), based on functional abstraction, e.g. truth table, decision diagrams or circuit abstraction, e.g. binary decision diagram (BDD), and-inverter graph (AIG) and majority inverter graph (MIG). These IRs play an important role in building circuits as the choice of an IR directly impacts on cost parameters of the design. In the authors' work, they are analysing the effects of different graph-based IRs (BDD, AIG and MIG) and their usability in making efficient circuit realisations.

M. Soeken et al., [6] presented a synthesis framework to map logic networks into quantum circuits for quantum computing. The synthesis framework is based on lookup-table (LUT) networks, which play a key role in conventional logic synthesis. Establishing a connection between LUTs in an LUT network and reversible single-target gates in a reversible network allows us to bridge conventional logic synthesis with logic synthesis for quantum computing, despite several fundamental differences.

V. Shukla et. al., [7] work presented two structure approaches for reversible acknowledgment of 8-bit adder-subtractor circuit with enhanced quantum cost. These plans are contrasted and existing structures on some selected performance parameters, for example, all out number of reversible gates, garbage outputs and quantum cost. The proposed plan for 8-bit adder-subtractor circuit utilizing reversible methodology reproduced utilizing Modelsim apparatus and blended for Xilinx Straightforward 3E with Gadget XC3S500E with 200 MHz frequency. This advanced circuit might be used further for the structuring of low power figuring gadgets.

GS Rajput et. al., [8] Number-crunching digital handling sub-frameworks are considered as one of the major segment of any electronic processing framework. The adder/subtractor circuit is one of the imperative piece of registering frameworks, for example, number juggling logic unit of any PC. Moreover, inclination of productive low misfortune preparing gadgets are the essential need of the time. This need is the essential inspiration for analysts to advance in the field of reversible circuit configuration approach. Low power VLSI circuits, DNA registering, optical figuring, signal preparing, quantum processing and nanotechnology and so on are a portion of the dynamic fields with the use of the reversible logic ideas.

K. Ghosh et. al., [9] Ternary quantum logic assumes an important job for structure fast and proficient advanced PCs. It has a few points of interest over old style processing and double quantum circuits. In this work, the acknowledgment of essential ternary circuits for adder/subtractor, encoder and priority encoder are proposed and structured. These circuits are fundamental for the development of different computational units of quantum PCs and other complex computational frameworks. Structure of reversible circuits can be improved by diminishing the quantum circuit cost. This work utilizes some rudimentary parts and run of the mill ternary gates (summed up ternary gate, M-S gate and so forth.) to perform number juggling expansion, subtraction and encoding tasks. At last, it assesses the ideal cost for each circuit.

M. Sangsefidi et. al., [10] Notwithstanding high mix thickness of QCA circuits, other one-of-a-kind determinations, for example, rapid and low power utilization urge scientists to use this innovation rather than CMOS innovation. In this work, another format of XOR gate is introduced in QCA innovation, at that point, it is abused to plan a 8-bit controllable inverter. At last, utilizing the proposed structure and last adder circuit given independent from anyone else in our past work, a 8-bit

adder/subtract or is planned. It is the most important segment of an ALU. All the structured circuits have utilized coplanar clock-zone based hybrid.

R. Bardhan et. al., [11] presented a productive adder/subtractor circuit utilizing QCA 3-dot cell. This model is very capable to register both expansion and subtraction tasks. it is additionally appeared here a solid subtractor circuit. Moreover, our new and novel plans has least number of QCA cells till now. The presented structures carry out more recipient than the present ones, e.g., the proposed 32-bit subtractor circuit improves 73% on QCA cell, 99% on territory and the proposed 32-bit adder/subtractor circuit improves 90% on QCA cell, 99% on region than the current best known one.

N. J. Lisa et. al., [12] presented the structure of quantum Ternary Peres Gate (TPG). The structure of our proposed quantum ternary adder/subtract or circuit comprises of two sections: a) Right off the bat, it has the plan of a quantum ternary full-adder circuit utilizing the proposed TPG gates, and b) Besides, it structures the proposed adder/subtract or circuit by utilizing the built full-adder in an) and M-S gates. it is additionally presented a heuristic to structure a minimal ternary adder/subtract or circuit.

III. CONVENTIONAL FULL ADDER CIRCUIT

A full adder is a fundamental building block in digital arithmetic circuits, widely used in processors and computational systems to perform binary addition. A full adder circuit is designed to add three one-bit binary numbers: two operands (A and B) and a carry input (Cin), producing a sum (S) and a carry output (Cout). This section provides a detailed overview of the structure, function, and operation of a conventional full adder circuit.
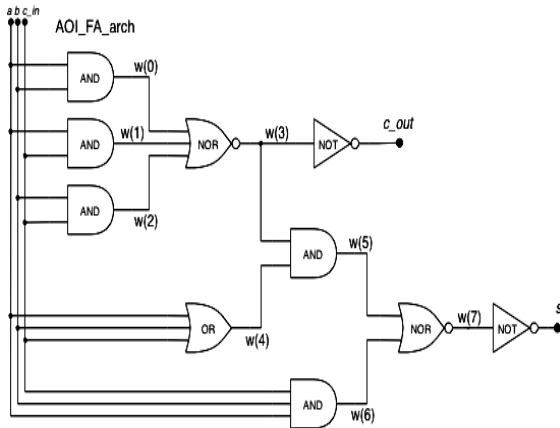
Figure 2: Full adder

Before proceeding further, the terms carry and sum should be clearly defined, which can be best done through an example. Consider the addition of the following decimal numbers: 5+6. When adding this decimal number, we cannot correctly represent the number "11" in the 1s place, so we carry a 1 to the 10s place, leaving a sum of 1 in the ones place. An equivalent process occurs for binary. When adding 1+1 in binary, you cannot represent "2" in the 1s place, so you carry a 1 to the 2s place, leaving a sum of 0. This is the case with the full adder. The sum (*s*) represents the remainder of the total sum *a+b+c_in*, after a carry (*c_out*) has been made, if necessary. The purpose of the full adder then is to find the sum of two 1-bit numbers and a 1-bit carry in.

The AOI_FA entity was written using dataflow, joining inputs with Boolean operators such as "and", "or" and "not." There is more than one way to construct the AOI_FA using VHDL dataflow descriptions. This project described each gate individually, connecting the output of one gate to the input of another using a wire. Alternately the outputs *c_out* and *s* could have been described as a combination of operators in a longer concurrent statement, reducing the number of internal wires needed.
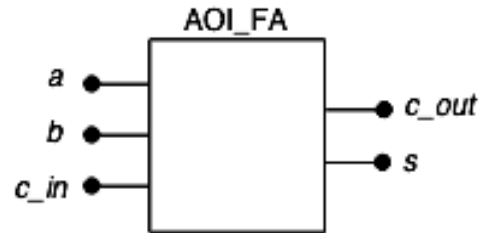

Figure 3: AOI_FA

After constructing the AOI_FA shown in Figure 4 using VHDL, we must test its function. Since there are three inputs to the entity, there are 2^3 unique combinations of inputs to test.

IV. CHALLENGES IN REVERSIBLE LOGIC

Some of the challenges in reversible logic is as followings-

1. Increased Circuit Complexity

One of the primary challenges in reversible logic design is the significant increase in circuit complexity compared to traditional irreversible circuits. Reversible logic circuits must maintain a one-to-one correspondence between inputs and outputs, which often requires more gates and additional logic elements to ensure that no information is lost.

- **Gate Overhead**: Reversible circuits generally require more gates than their irreversible counterparts to perform the same function. This can lead to an increase in the overall circuit size, making it difficult to optimize for both area and power efficiency.

- **Ancilla Inputs and Garbage Outputs**: To maintain reversibility, reversible circuits often require the use of **ancilla inputs** (constant inputs) and **garbage outputs** (unwanted outputs that are necessary for reversibility but do not contribute to the final result). These extra inputs and outputs add complexity and reduce the overall efficiency of the circuit.

2. Quantum Cost

The **quantum cost** of a reversible circuit refers to the number of elementary quantum operations (such as CNOT gates or Toffoli gates) needed to implement the circuit. While

reversible logic is a key enabler for quantum computing, minimizing the quantum cost of reversible circuits is a major challenge, especially for complex operations like addition and subtraction.

- **Complex Gate Decompositions**: Many reversible gates, such as the Toffoli and Fredkin gates, must be decomposed into simpler quantum gates when implemented in a quantum computer. This increases the quantum cost and can introduce delays, making it challenging to design efficient, high-speed reversible circuits.

- **Gate Depth and Latency**: The gate depth (the longest path between any two gates) directly impacts the speed of the circuit. Minimizing gate depth is crucial for achieving high-speed arithmetic operations, but this is often difficult due to the complexity of reversible circuit designs.

3. Delay and Carry Propagation

In traditional arithmetic circuits, carry propagation is a major factor in determining the speed of addition and subtraction operations. Reversible logic-based arithmetic circuits face similar issues, particularly when implementing reversible carry-lookahead adders (CLAs) or other advanced adder architectures.

- **Carry Propagation Delay**: Reversible circuits, like irreversible ones, must address the issue of carry propagation in addition operations. Designing reversible circuits that minimize the delay associated with carry propagation, while maintaining reversibility, is a complex task.

- **Optimizing Reversible CLAs**: Carry-lookahead adders are commonly used in traditional circuits to reduce delay, but implementing these efficiently in a reversible logic framework is challenging due to the increased gate count and complexity.

4. Power Efficiency Trade-offs

While reversible logic theoretically offers power efficiency benefits by avoiding information loss, practical implementations often face trade-offs between power savings and other performance metrics like speed and area.

- **Overhead from Ancilla and Garbage Outputs**: The need for ancilla inputs and garbage outputs in reversible circuits can offset some of the power savings gained from reversibility. The extra logic required to manage these inputs and outputs can lead to higher power consumption and area overhead, which is especially problematic in large-scale circuits.

Energy Efficiency in Physical Implementations: Achieving true energy efficiency in reversible circuits requires careful optimization at both the design and physical implementation levels. In practice, the energy savings may be less significant than theoretical predictions due to the additional resources required to ensure reversibility.

V. CONCLUSION

Reversible logic has become one of the most promising research areas in the past few decades and has found its applications in several technologies; such as low power CMOS, nano-computing and optical computing. Reversible logic gates are widely known to be compatible with future computing technologies which virtually dissipate zero heat. This paper reviews of the reversible realization of adder-subtractor circuits. The lowest level entities, XOR_GATE and AOI_FA, were described using the dataflow method. These entities were combined together using the structural description method to make a 1-bit adder/subtractor, which was repeated and ultimately created the 8-bit adder/subtractor.

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