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VLSI Implementation of Orthogonal Matching Pursuit for FPGA-DSP Application

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***Abstract*— Orthogonal Matching Pursuit (OMP) is a widely used algorithm for sparse signal recovery. It is an iterative algorithm that solves the problem of finding the sparsest solution of an underdetermined linear system. OMP provides an efficient and effective way to find the sparsest solution of an underdetermined linear system by iteratively selecting the most correlated columns of a dictionary matrix that are most likely to contribute to the sparse solution. This paper presents the study of VLSI implementation of the Orthogonal Matching Pursuit (OMP) for high-speed FPGA Application. Simulation is performed using the Xilinx 14.7 software.**

***Keywords*— OMP, Signal Recovery, FPGA-VLSI.**

I. INTRODUCTION

Orthogonal Matching Pursuit (OMP) is an iterative algorithm for signal processing applications that aims to find the best sparse approximation of a signal. It is a computationally efficient and widely used algorithm in various fields, including image processing, audio signal processing, and machine learning. In recent years, there has been increasing interest in implementing OMP on field-programmable gate arrays (FPGAs), due to their parallel processing capabilities and reconfigurability. PGAs are reconfigurable hardware devices that offer high parallelism and low latency, making them well-suited for signal processing applications. FPGA-based implementations of OMP have been proposed to achieve high computational efficiency and low power consumption.

There are two main approaches to implementing OMP on an FPGA: a software-defined radio (SDR) approach and a hardware accelerator approach.

The SDR approach involves implementing the OMP algorithm using a software-defined radio framework, such as GNU Radio. The framework provides a high-level programming interface for designing and implementing signal processing algorithms on FPGAs. The OMP algorithm is implemented using blocks or modules that are interconnected to form a signal processing pipeline.

The SDR approach has the advantage of being flexible and adaptable to different signal processing applications. However, it may not be as efficient as a dedicated hardware implementation, as the OMP algorithm is implemented using generic building blocks that may not be optimized for OMP specifically.

The hardware accelerator approach involves designing a dedicated hardware accelerator for the OMP algorithm. The accelerator is implemented using hardware description languages (HDLs), such as Verilog or VHDL, and is optimized for OMP specifically.

The hardware accelerator approach has the advantage of being highly efficient and low power, as the hardware is optimized for the specific requirements of the OMP algorithm. However, it may be less flexible and adaptable to different signal processing applications, as the accelerator is designed specifically for OMP.

II. METHODOLOGY

The present work methodology can be understand using the following flow chart-

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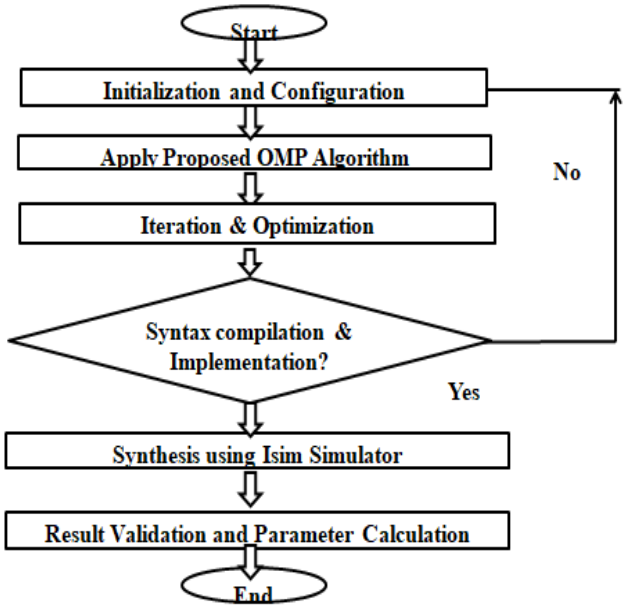

Figure 1: Flow chart

Step-1: Assign various constant, variable and configuration for initialization of simulation process.

Step-2: Implement Orthogonal Matching Pursuit algorithm.

Step-3: Now iteration process starts and its continue till the optimization.

Step-4: Now syntax compilation & implementation process then it Generate Register transfer level view and all internal logic circuits.

Step-5: Result validation through xilinx test bench with Isim simulator, Simulation parameters calculation and comparison.

OMP implementation generally receives measurement matrix and measured vector as inputs, which results in the output of an estimation of as the approximation value of the original signal.

The OMP algorithm can be expressed mathematically as follows:

- Initialization: Set the residual r_0 to be the input signal y, and initialize an empty set S of selected basis vectors.
- Selection: For each iteration k, select the basis vector a_j that maximizes the correlation between the residual r_{k-1} and the basis vector a_j, i.e.,

j_k = argmax_{j} |<a_j, r_{k-1}>|

where <a_j, r_{k-1}> denotes the inner product between a_j and r_{k-1}.

Add the selected basis vector a_{j_k} to the selected set S.

- Projection: Let A_S be the submatrix of the dictionary A consisting of the columns corresponding to the selected basis vectors in S. Compute the coefficients c_S by solving the following linear system:

c_S = argmin_{x} ||y - A_S x||_2

where ||.||_2 denotes the L2 norm.

- Termination: The algorithm terminates when either a desired sparsity level is reached, i.e., |S| = k, or the residual becomes sufficiently small, i.e., ||r_k||_2 < epsilon.

III. SIMULATION AND RESULTS

The simulation work is performed using the Xilinx ISE 14.7 software. The simulated results is as followings-

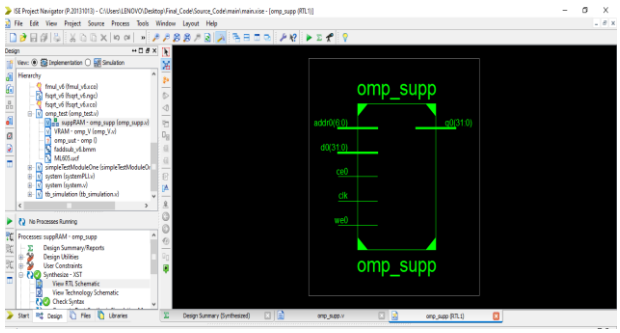

Figure 2: Top module

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Figure 2 is indicating top module of proposed orthogonal matching pursuit.

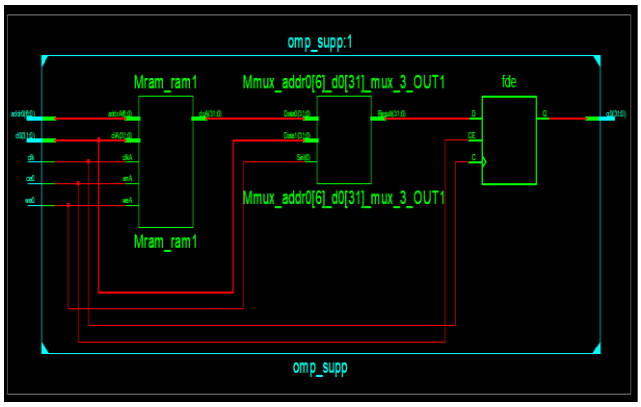

Figure 3: Internal circuit

Figure 3 is presenting internal circuit view of OMP, it includes memory RAM, add, mux etc blocks.

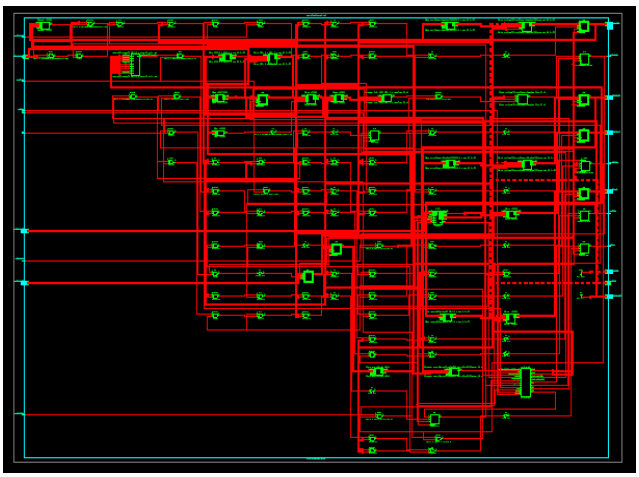

Figure 4: Technological view

Figure 4 is presenting the technological view of test module of OMP

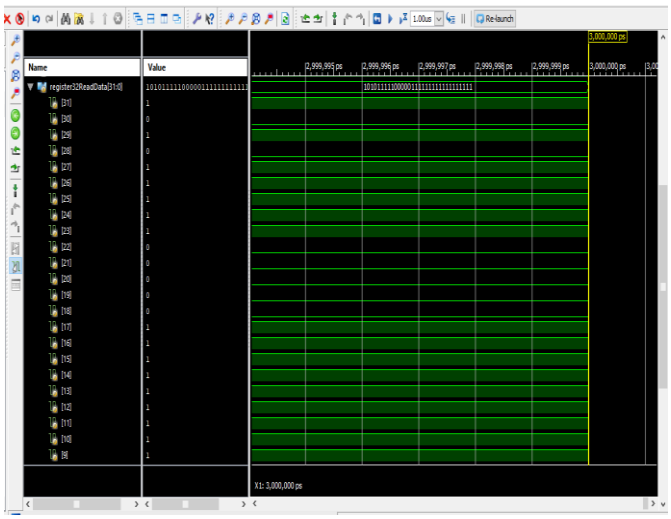

Figure 5: Memory Read data

The correlation computation involves reading data from the memory and performing matrix operations. To optimize the memory access, it is common to use a block-based matrix representation, where each column of the dictionary matrix is stored in a separate memory block.

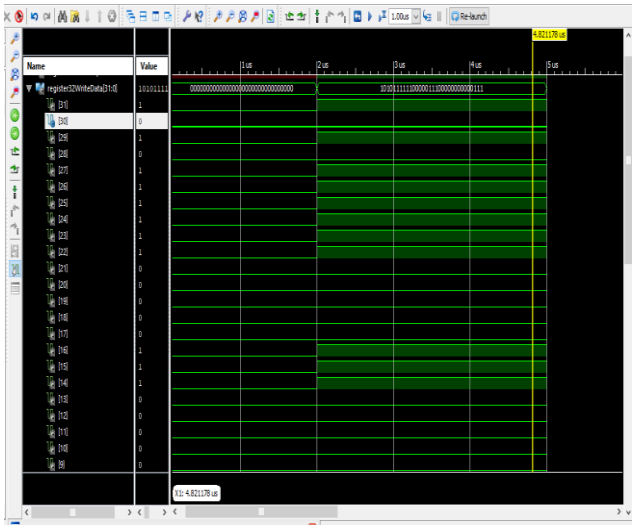

Figure 6: Memory Write data

To optimize the memory, write operations, it is common to use a block-based matrix representation, similar to the memory read operations. Each block of the dictionary matrix is associated with a separate array of projection coefficients,

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and the coefficients are written to the corresponding array during the computation.

Table 1: Result Comparison

Sr no.	Parameter	Previous design [1]	Proposed Design
1	Frequency	113 MHz	483 MHz
2	Latency	15.2 ns	2.07 ns
3	LUT	440	116
4	Flip-Flop	596	61
5	Speed or Throughput	6.5 GHz	15.4 GHz

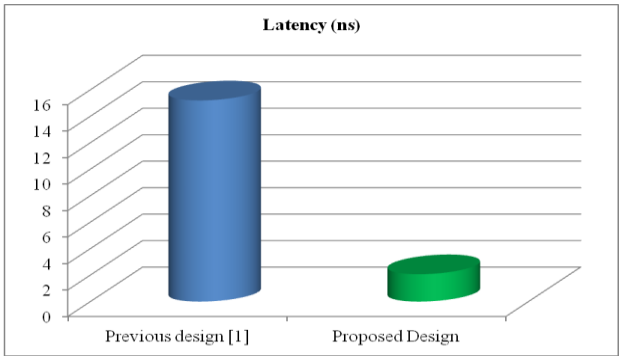

Figure 7: Comparison- Latency

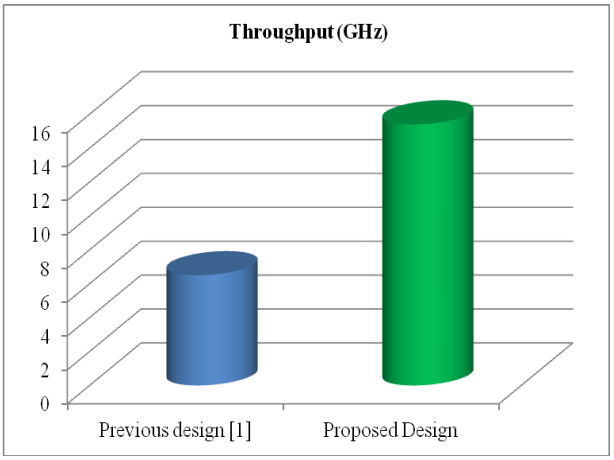

Figure 8: Comparison- Throughput

IV. REFERENCES

This paper presents the study of VLSI implementation of orthogonal matching pursuit for FPGA-DSP application. The proposed OMP achieved the value of frequency is 483MHz while previous it is 113MHz, the latency is 2.07ns while previous it is 15.2ns. The look up table used by the proposed OMP is 116 while previous it is 440, The flip flop pair is 61 while previous it is 596. The total speed or throughput is 15.4GHz by the proposed work while previous it is 6.5GHz. Therefore, it is clear from the simulated results; the proposed OMP provides the significant better results than the previous work.

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